SIV100B

1/7-INCH VGA CMOS IMAGE SENSOR
WITH IMAGING SIGNAL PROCESSOR

SEOUL ELECTRONICS & TELECOM
SENSOR DIVISION

1. Overview

1.1. General Description

The SIV100B features 640V x 480H resolution with 1/7-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC, and embedded image signal processor.
The full scale integration of high-performance and low-power functions makes the SIV100B best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

The SIV100B performs a huge range of on-chip image processing functions of auto exposure, auto white balance, black level compensation, 5x5 matrix interpolation, false color correction, gamma correction, color correction, lens shading correction and so on. It delivers optimized and superb image quality with greater flexibility to designers.

It incorporates on-chip camera functions of sub-sampling, windowing that generates such various output size formats as VGA, CIF and output data formats as Bayer RGB, and YCbCr formats. Those advanced features including X/Y image flip and color effect can be easily controlled and programmed through a simple I2C interface.

1.2. Applications

- Cellular phones
- PDAs
- PC/Dual-mode cameras

2. Contents

3. Features

- 0.18um CMOS Process Technology
- Micro-lens for high Sensitivity and RGB Mosaic Color Filter Array
- Pipeline 10bit integrated Analog-to-Digital Conversion
- Power Sleep(Idle) & Down Mode for Power Saving
- VGA, CIF, Sub-sampling Mode, and programmable User Window Size
- YUV/YCbCr 422, and 8bit RGB Bayer Output Data Formats
- Power Supply Voltage : 2.4V~2.9V/1.6V~2.0V
  (2.4V~2.9V for Analog, 1.8V ~ 2.9V for I/O Power, 1.6V~2.0V for Digital Core)
- I2C Serial Programming Interface
- Progressive Scan Mode & Electronic Rolling Shutter
- Integrated on-chip Image Digital Processing
  Automatic Exposure (AE)
  Automatic White Balance (AWB)
  Automatic Band Filter (Auto Anti-Flicker) : 50Hz/60Hz Flicker Automatic Cancellation
  Automatic Gain Control (AGC)
  Black Level Compensation (BLC)
  5x5 Color Interpolation
  False Color Correction
  Lens Shading Correction
  FPN, Horizontal/Vertical Line, and Random Noise Cancellation
  Gamma Correction
  Color Correction - 3x3 Color Matrix & Color Space Conversion (CM & CSC)
  Hue / Sharpness / Brightness / Contrast Stretch / Saturation Control
  Color Effect – Sepia,Mono,Inverted Mono,Emboss,Sketch
  Zooming (Sub-Sampling) & Windowing
  Image X/Y Flip

4. Key Specifications

Table 1. Key specifications

Parameter		Typical Value
Optical Format		1/7-inch
Pixel Size		3.2um x 3.2um
Image Area		2.08mm (H) x 1.57mm (V), 2.61mm Diagonal
Video Format		640H x 480V
Effective Pixel Array		652H x 492V
Total Pixel Array		668H x 533V
Output Data Format		YUV/YCbCr 422, and 8bit RGB Bayer
Output Display Format		VGA(640x480), CIF(352x288) User Define Window
ADC Resolution		10bit ADC
Sensitivity		1.7 V/Lux-Sec
Maximum Frame Rate		30fps @ VGA, 27MHz MCLK
Maximum Master Clock		27MHz
Operating Temperature		-30~70℃
Dynamic Range		55 dB
SNR		42 dB
Dark Signal		15 mV/Sec
Supply Voltage	Core	1.6V ~ 2.0V
	Analog	2.4V ~ 2.9V
	I/O	1.8V ~ 2.9V
Power Consumption		50mW @ 30fps, VGA 10uA @ Stand-by
Package-Type		48-CLCC, COB, COF

5. Block Diagram

Figure 1. Block diagram

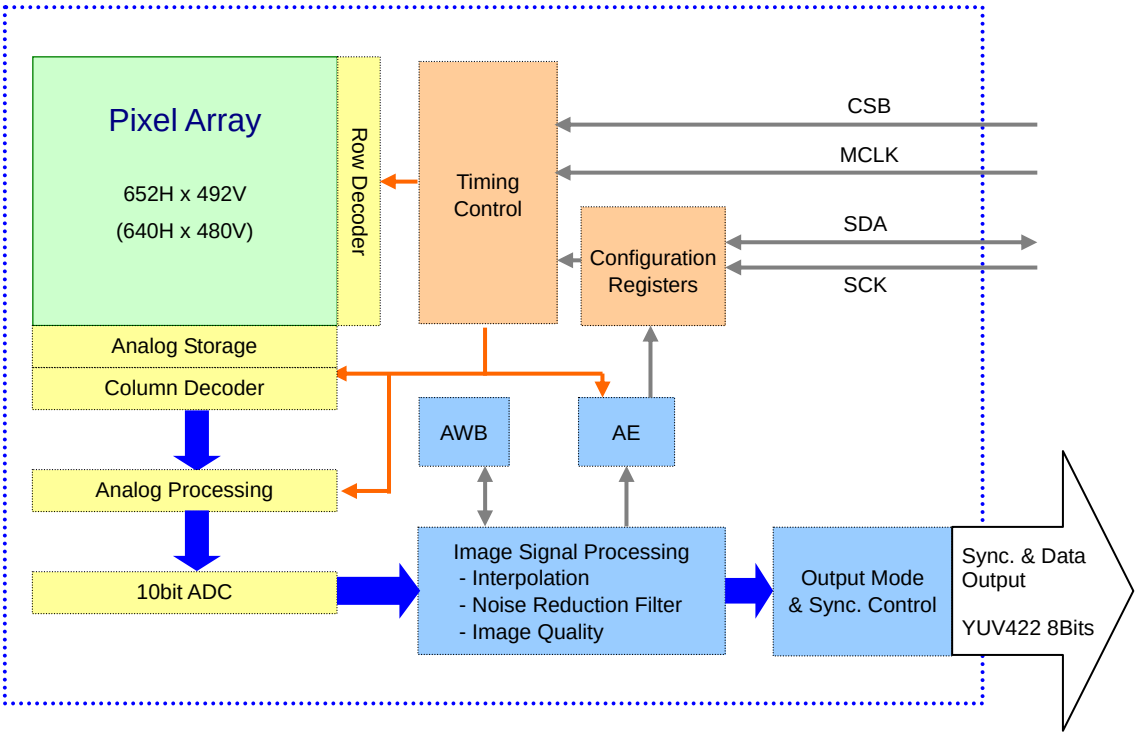
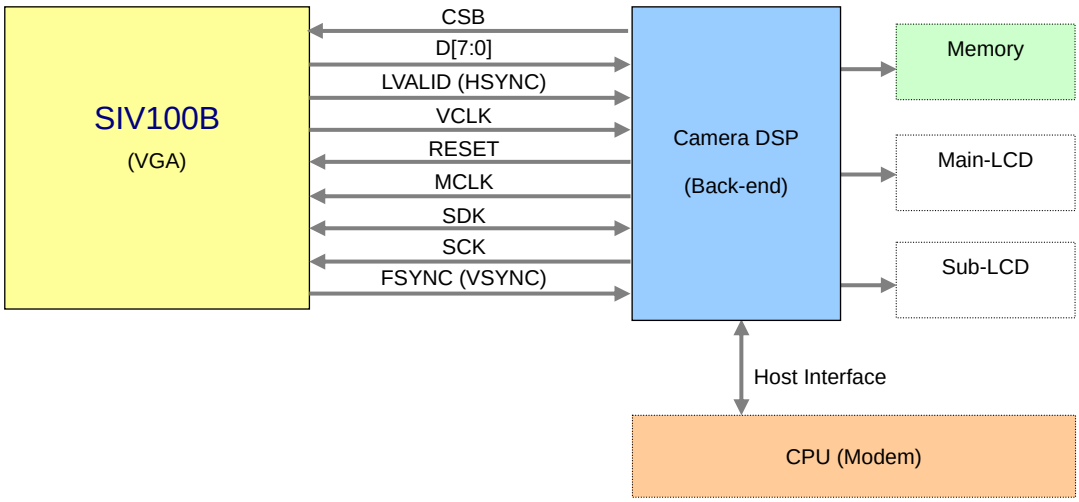


Figure 2. System interface



6. Pin Description

Figure 3. Pad information

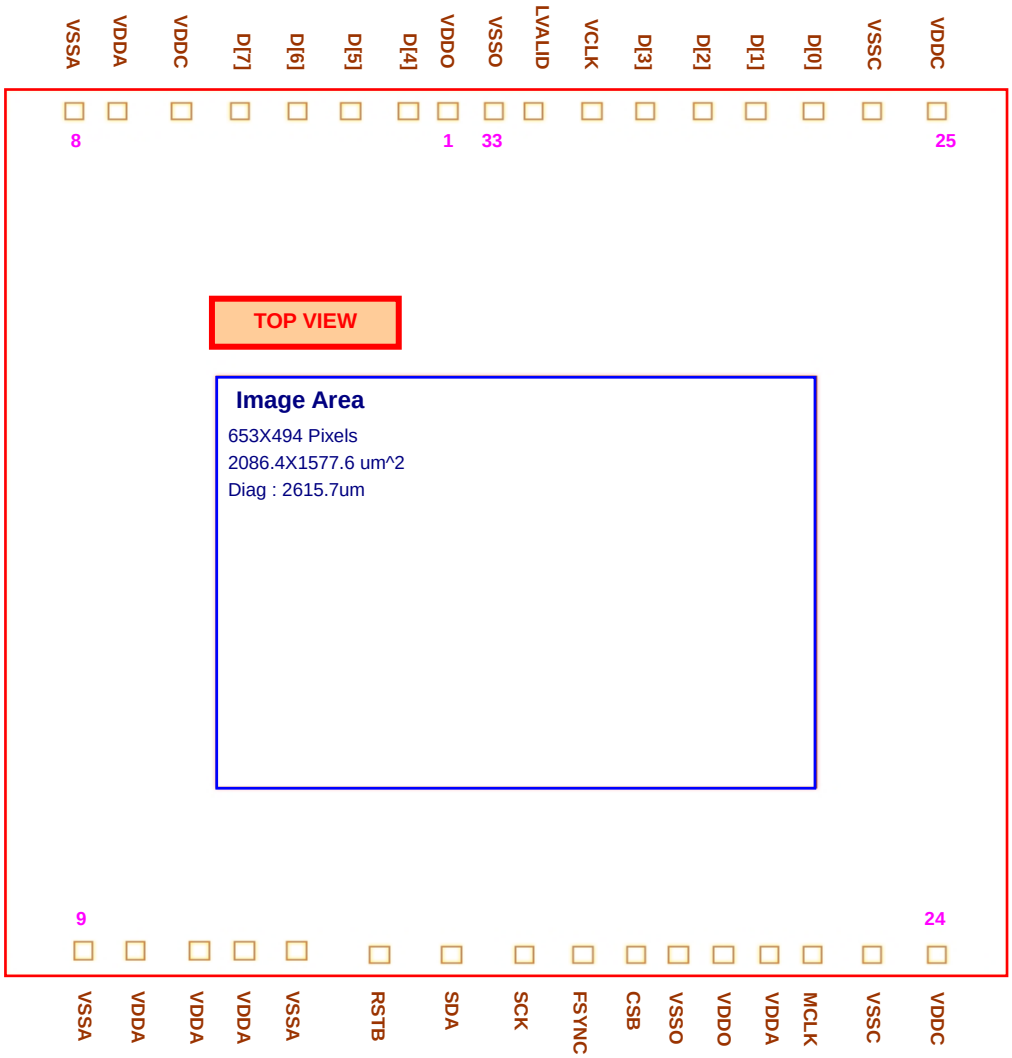


Table 2. Pin description

Pin No.	Pin Name	Pin Description	Pin Type
1	VDDO	Digital IO Power (1.8V~2.9V)	Power supply
2	D[4]	Data Out[4]	Tri-Output
3	D[5]	Data Out[5]	Tri-Output
4	D[6]	Data Out[6]	Tri-Output
5	D[7]	Data Out[7]	Tri-Output
6	VDDC	Digital Core Power 1.8V	Power supply
7	VDDA	Analog Power (2.8V)	Power supply
8	VSSA	Analog Ground	GND
9	VSSA	Analog ASP, REFERENCE. PGA. Ground	GND
10	VDDA	Analog ASP. Power 2.8V	Power supply
11	VDDA	Analog REFERENCE. Power 2.8V	Power supply
12	VDDA	Analog PIXEL. Power 2.8V	Power supply
13	VSSA	Analog PIXEL. Ground	GND
14	RSTB	RESET, Active Low	Input
15	SDA	IIC-Bus Serial Data Line	Bi-directional
16	SCK	IIC-Bus Serial Clock Line	Input
17	FSYNC	Vertical synchronization	Tri-Output
18	CSB	Chip enable, Active Low	Input
19	VSSO	Digital IO Ground	GND
20	VDDO	Digital IO Power (1.8V~2.9V)	Power supply
21	VDDA	Analog Power 2.8V	Power supply
22	MCLK	MCLK	Input
23	VSSC	Digital Core Ground	GND
24	VDDC	Digital Core Power 1.8V	Power supply
25	VDDC	Digital Core Power 1.8V	Power supply
26	VSSC	Digital Core Ground	GND
27	D[0]	Data Out[0]	Tri-Output
28	D[1]	Data Out[1]	Tri-Output
29	D[2]	Data Out[2]	Tri-Output
30	D[3]	Data Out[3]	Tri-Output

Pin No.	Pin Name	Pin Description	Pin Type
31	VCLK	Output Pixel Data Synchronous Clock	Tri-Output
32	LVALID	Data Valid Indicator Signal	Tri-Output
33	VSSO	Digital I/O Ground	GND

7. Pixel Array Information

The sensor core pixel array is configured as 668 columns by 533 rows. In default mode a VGA image (640 columns by 480 rows) is generated, starting at red pixel of column 8, row 20. CIF image squeezes 364 columns by 300 rows out of VGA optically active pixel array by windowing.

Figure 4. Pixel array structure

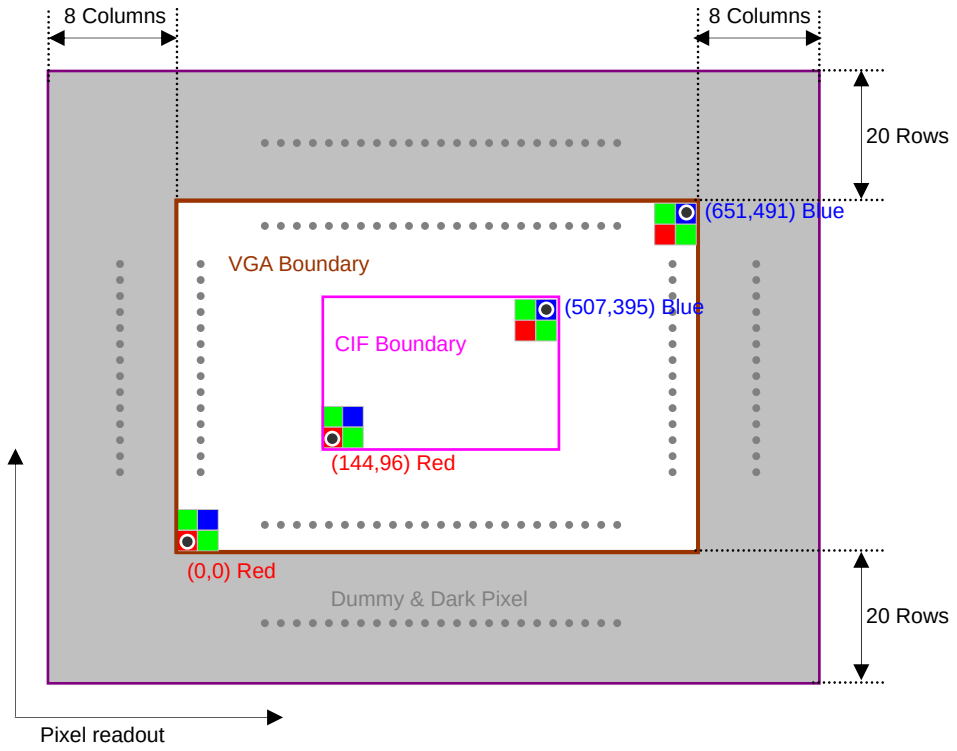


Table 3. Pixel coordinates

Video format	Window size	Pixel coordinates	Remark
Total pixel array	668H x 533V		Dummy & dark pixels
VGA	652H x 492V	(0, 0) ~ (651, 491)	
CIF	364H x 300V	(144, 96) ~ (507, 395)	

8. Timing Guide

8.1. Chip Selection

SIV100B supports the chip select function for dual mode. If CSB state is high, chip is entered to reset mode and any functions can not operate. The reset sequence is begun after CSB state is low.

8.2. Relation of Clocks

The PCLK that is the pixel operation clock for internal circuit, and is mostly used for the internal operation, and timing controls like a frame timing control, integration timing control, and so on.
The CLK_DIV function of the CNTR_B[3:2] register can define the PCLK frequency examples as follows.

Table 4. Table 3. The PCLK interrelation as per the CLK_DIV function

CLK_DIV[1:0]		PCLK
B3	B2	
0	0	1/2 MCLK Frequency
0	1	1/4 MCLK Frequency
1	0	1/8 MCLK Frequency
1	1	1/16 MCLK Frequency

The VCLK that is the pixel output clock for external circuit to synchronize D[7:0] differs accordingly to the display modes and video output formats.

Table 5. The VCLK change as per every different display modes and formats

Video Display Mode	VCLK	
	Bayer	YCbCr
VGA	PCLK	2 PCLK
CIF	PCLK	2 PCLK

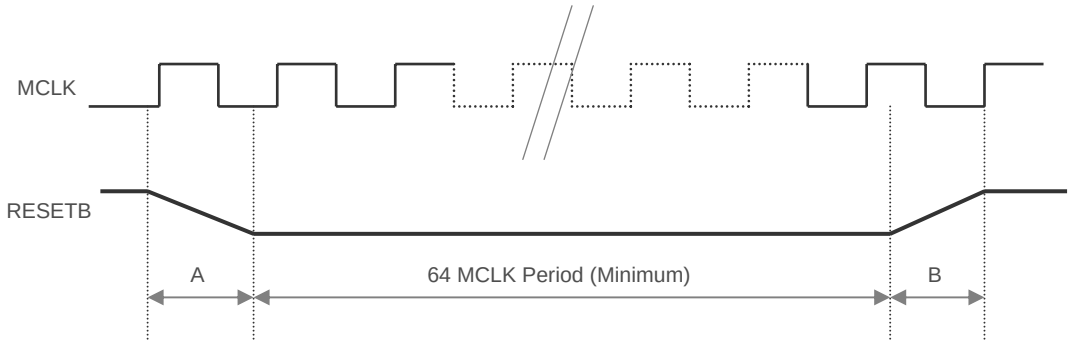
8.3. Reset Sequence

The reset sequence should be triggered through the RESETB and MCLK pins before the sensor is turned on.

The initialization of the sensor reset is begun when the RESETB pin goes from high to low level, and it is required that reset period is holding for more than 64 MCLK clocks while the RESETB pin keeps its active low condition. The falling time (A) and rising time (B) are not considered herein.

All of the reset procedure is terminated as all internal registers are loaded by each default value, and sensor becomes stable.

Figure 5. Figure 4. Reset of the sensor



8.4. Power-down Mode

When the CNTR_A[1] is enabled(1) and I2C power-down mode can be activated, internal clocks are turned off, and all internal digital and analog blocks go into an inactive mode except I2C. Along with this, the power consumption is reduced considerably.

The input MCLK and VDD don't have specific effects on the power-down mode operation, therefore don't need to be controlled by the power-down scheme at the system. As long as the input clock remains on, the chip will allow accesses through the serial interface.

In order to wake the power-down mode, only to assert the CNTR_A[1] to be disabled(0).

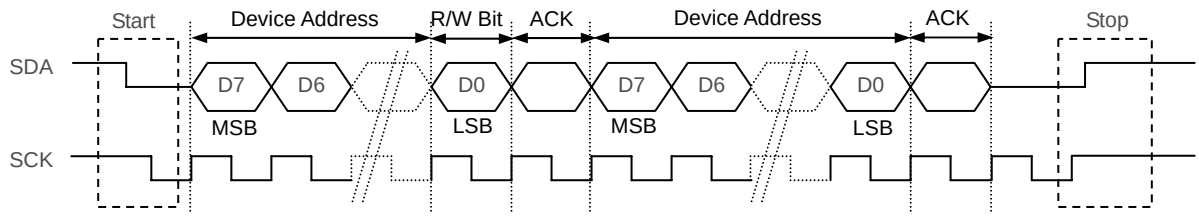
8.5. I2C Control

The internal registers of the sensor are programmable through I2C serial bus interface that has SDA(Serial Bus Data, Bi-directional) and SCK(Serial Bus Clock, Input) pins, and can be used to write and read the required data into. The sensor can operate only as a slave.

MCLK should be supplied and RESETB high, before programming the two-wire serial bus interface.

The I2C device address of the sensor is 0x33, therefore it can be actually programmed by R/W operations into the 0x66/0x67 addresses.

Figure 6. Two-wire serial bus interface



The logical transition of the SDA from high to low level drives its start condition, and from low to high asserts its stop condition of its serial interface programming while the SCK is at high state. Every byte of 8 bits transferred to the bus should be followed by an Acknowledge, and the most significant bit of the byte should always be transmitted first.

The R/W programming is set by single or multiple byte operation. The register address of the sensor is automatically incremented by 1 in a multiple byte mode. If there is more data to read, the SDA should be driven to a low state and data read sequence from register address is repeated. Otherwise, the SDA must be pulled high to end the read transaction.

The herebelow figures show the detailed examples of each I2C sequence.

*ACK1 : Acknowledge from the sensor

0 : Valid

1 : Invalid

* ACK2 : Acknowledge from the master device

0 : There are more data to read

1 : No more data to read

Figure 7. Figure 7. Register write sequence of single byte operation

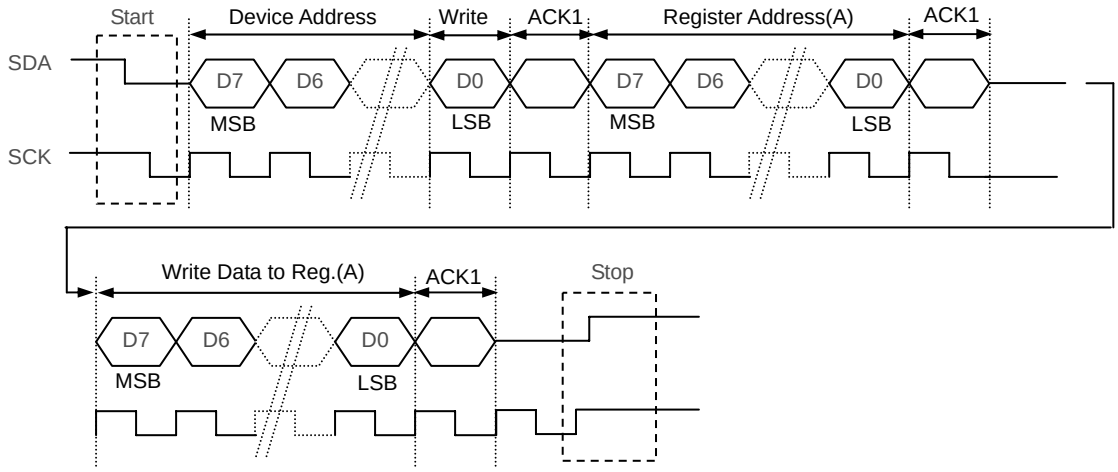


Figure 8. Register write sequence of multiple byte operation

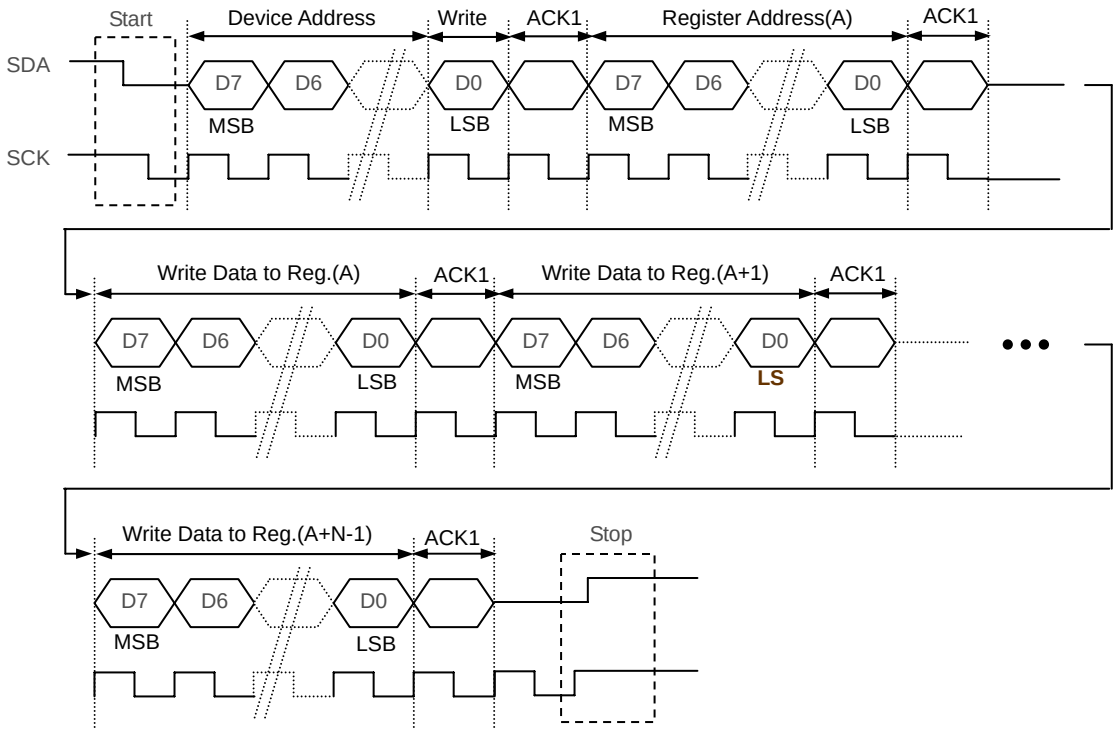


Figure 9. Register Read sequence of single byte operation

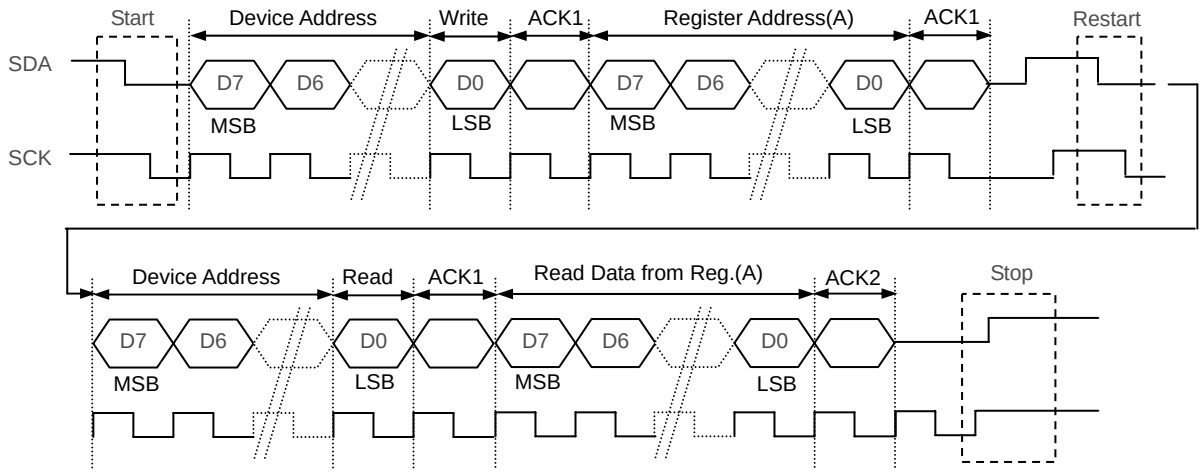
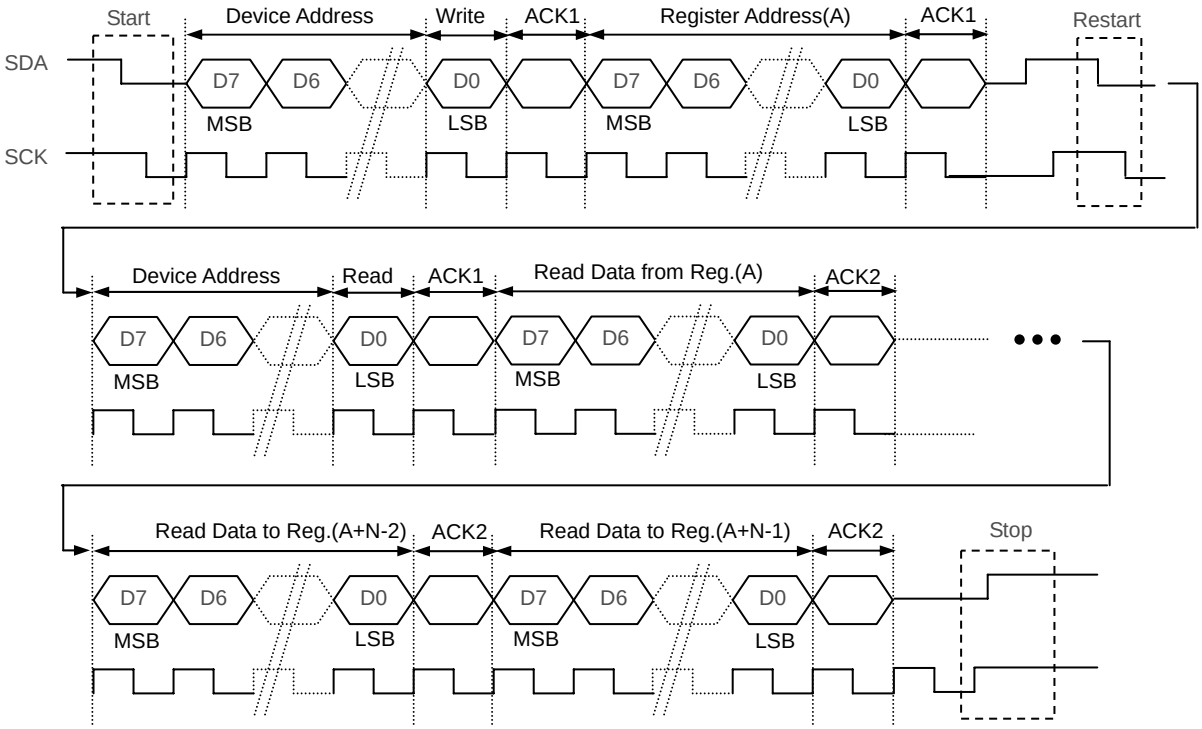


Figure 10. Register Read sequence of multiple byte operation



8.6. Frame Timing Information

A frame size including horizontal and vertical blanking, valid image data is synchronized with the PCLK, internal pixel clock. The amount of horizontal and vertical blanking is achieved by programming the bits in corresponding registers as described herebelow.

Table 6. Related register

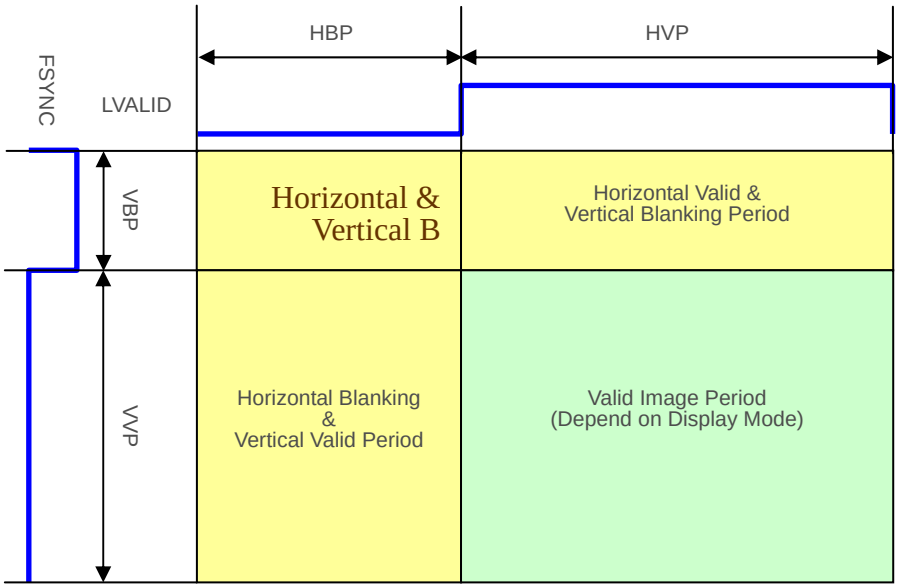
Register	Address	Description
VMODE	0x05	Video mode control register
BNKT60	0x20	Frame time control register
HBNKT60	0x21	Frame time control register
VBNKT60	0x22	Frame time control register
BNKT50	0x23	Frame time control register
HBNKT50	0x24	Frame time control register
VBNKT50	0x25	Frame time control register

Table 7. Frame timing combination

AC Frequency	Vertical Blanking Reg.	Horizontal Blanking Reg.
60MHz	BNKT60[1:0], VBNKT60[7:0]	BNKT60[5:4], HBNKT60[7:0]
50MHz	BNKT50[1:0], VBNKT50[7:0]	BNKT50[5:4], HBNKT50[7:0]

8.6.1. Frame Timing Description

Figure 11. Frame timing



1 Frame Period = ((HBP+HVP)x(VBP+VVP))x1 PCLK Period

(1) HBP (Horizontal Blanking Period)

> HBP=(HST+HBNKT60/50 register value+1)x1 PCLK

> HBNKT60/50[9:0]={BNKT60/50[5:4], HBNKT60/50[7:0]}

> HST(Horizontal Scan Time) : 149 PCLKs

(2) HVP (Horizontal Valid Period)

> Its value depends on a display mode.

> VGA Mode : 650 PCLKs / CIF Mode : 362 PCLKs

(3) VBP (Vertical Blanking Period)

> VBP=(EVBP+VBNKT60/50 register value+1)x1 Row

> VBNKT60/50[9:0]={BNKT60/50[1:0], VBNKT60/50[7:0]}

> EVBP(Extra Vertical Blanking Period) : 10-line default

It can be possible to be changed into 4-line by users. But, it is needed to discuss with SET for more information in this case.

(4) VVP (Vertical Valid Period)

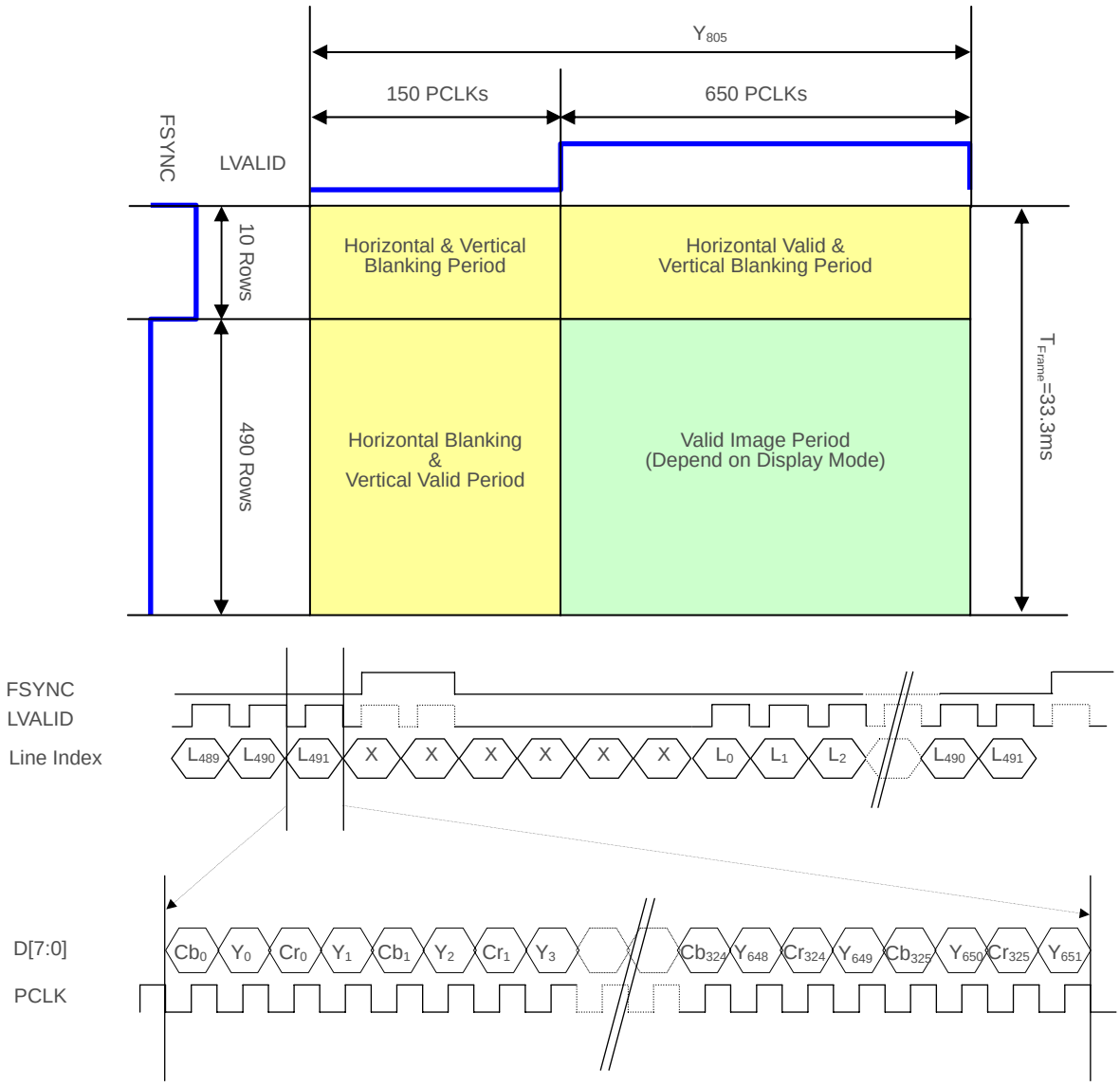
> Its value depends on a display mode.

> VGA Mode : 492 lines / CIF Mode : 300 lines

8.6.2. Default Window Configuration

Register setting shows VGA YCbCr 422 output format through 8-bit image data as below. Its frame rate and frame period are achieved as per programmed pixel array and timing.

Figure 12. Default window configuration for VGA YCbCr 422 format output at 24MCLK

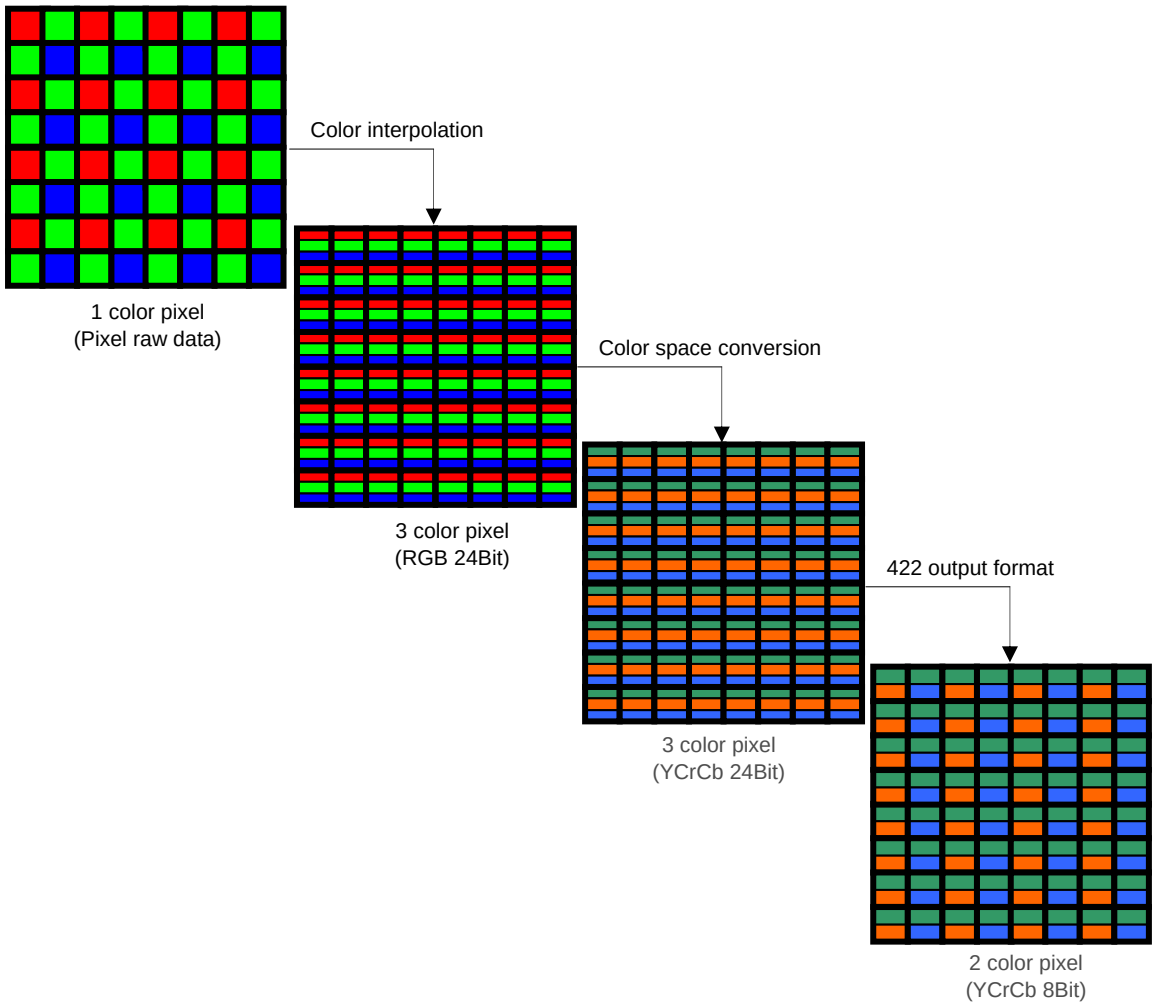


9. Functional Description

9.1. Video Output Format Information

Pixel array has Bayer mosaic color filters, and each pixel has only one type of color filter on it. As it is necessary to get all of RGB color components to assert a full color for a pixel, missed data must be inferred from color data of other pixels by color interpolation. Since human eyes are less sensitive to color variations than luminance, each color component can be sub-sampled to reduce the amount of data to be transmitted, but almost preserve the same image quality.

Figure 13. Video output format conversion



Each pixel consists of two data of Y, Cr, or Y, Cb, and its data output order can be programmed by setting OUTFMT[5:4] register, in the 8-bit YCbCr 422 output format as shown below.

Table 8. YCbCr output order

OUTFMT[5:4]	Output order	Remark
00	Cr → Y → Cb → Y	C First & Cr First
01	Cb → Y → Cr → Y	C First & Cb First
10	Y → Cr → Y → Cb	Y First & Cr First
11	Y → Cb → Y → Cr	Y First & Cb First

9.2. Video Output Size Information

9.2.1. Video size by sub-sampling and zooming

The CNTR_C registers are accessible to set a variety of the display image sizes as below. These display video sizes are deeply related to their data output format.

Table 9. Video output size

VMODE[2:0]			Video format	Video Output Size
D2	D1	D0		
0	0	0	QQCIF	88 x 72
0	0	1	QCIF	176 x 144
0	1	0	CIF	352 x 288
0	1	1	CIF	352 x 288
1	0	0	QQVGA	160 x 120
1	0	1	QVGA	320 x 240
1	1	0	VGA	640 x 480
1	1	1	VGA	640 x 480

9.2.2. Sub-sampling

Each 2 rows and columns at every sub-sampling mode are picked out from RGB Bayer output

data by 1/2, and 1/4 sub-sampling method herebelow. It takes only 1/4 frame periods of the full resolution case so that the frame rate of each video formats are 4 times increased accordingly.

Figure 14. 1/2 sub-sampling

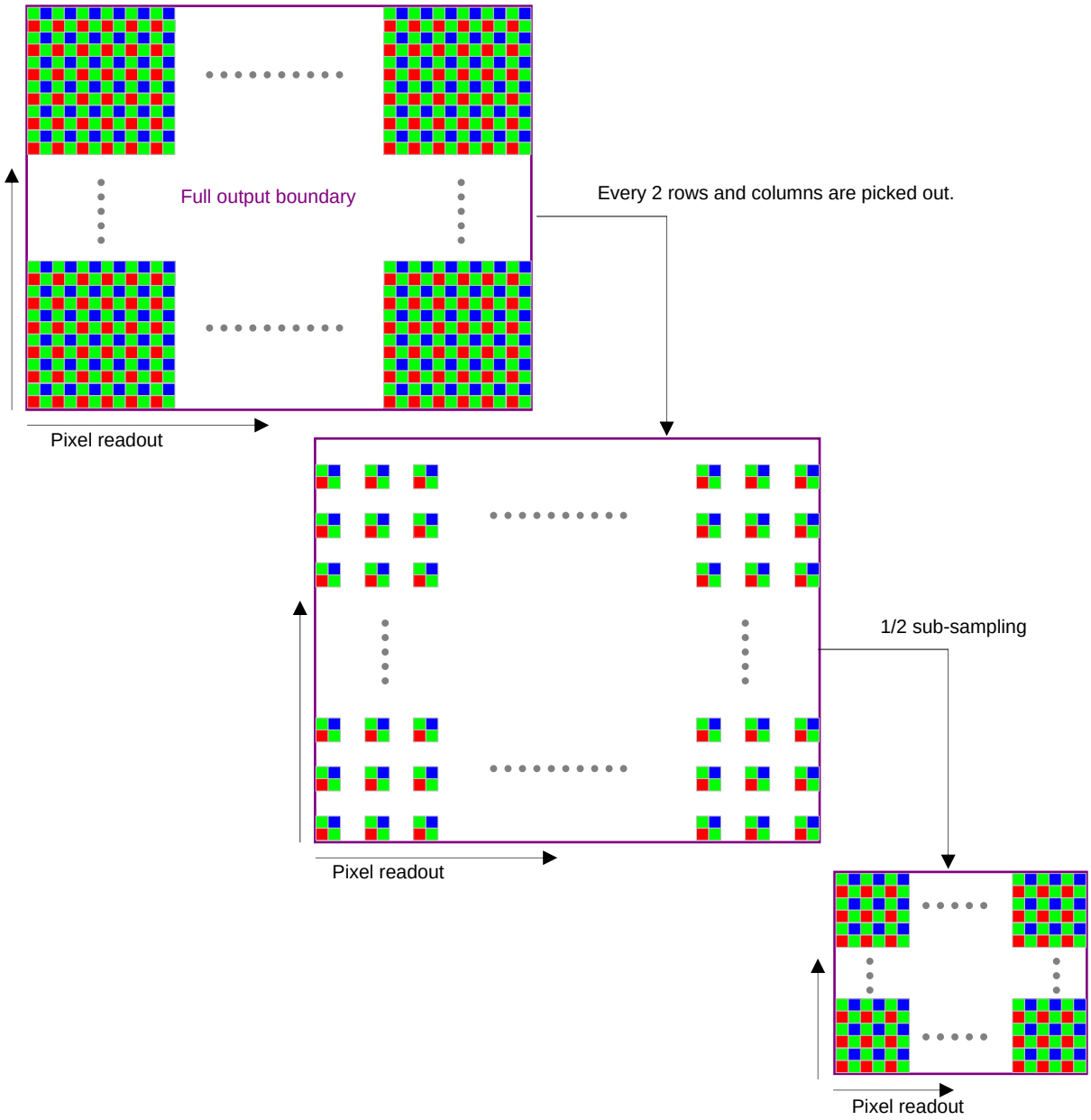
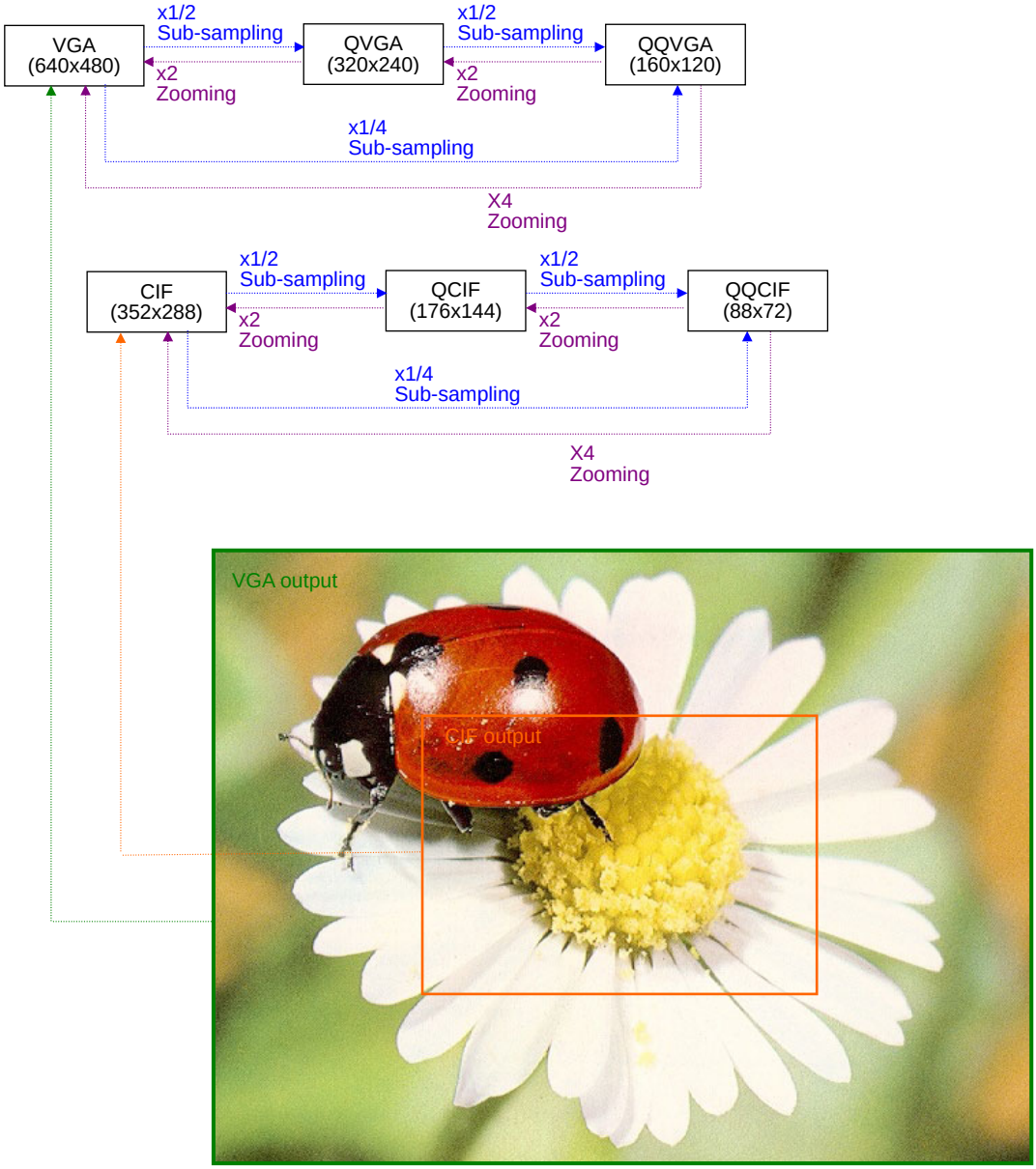


Figure 15. Sub-sampling and zooming



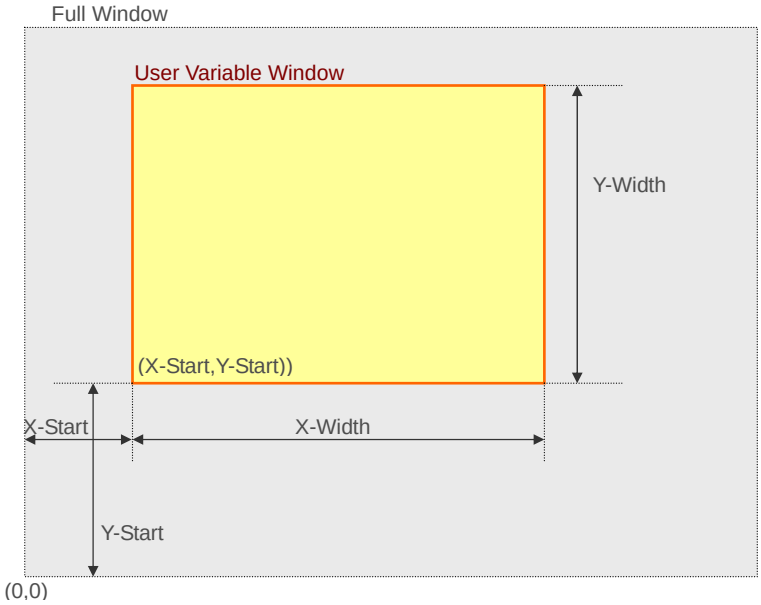
9.2.3. Video size by user variable windowing

The window starting position and size of the frame is determined by asserting user variable windowing function, and programming registers hereafter. Original position(0,0) of the frame is at the down left corner, and each line scan direction is from left to right. One frame consists of vertical width+1 column, and horizontal width+1 row. The full window and user variable window is triggered by enabling the WINEN bit of the OUTFMT[3] register.

Table 10. Related registers

Register	Address	Description
OUTFMT	0x82	Output Format Control
WDATH	0xF0	Window Data High Byte
WHSRTL	0xF1	Window Horizontal Start Low Byte
WHWIDL	0xF2	Window Horizontal Width Low Byte
WVSRTL	0xF3	Window Vertical Start Low Byte
WVWIDL	0xF4	Window Vertical Width Low Byte

Figure 16. User variable window



9.3. X/Y-Flip Image and Data Readout Order

The pixel data are read out from left to right in horizontal direction, and from bottom to top in vertical direction normally. By changing the mirror mode, the read-out sequence can be reversed and the resulting image can be top in vertical mirror mode. The horizontal and vertical mirror mode can be programmed by X/Y-flip control register, CNTR_B[1:0]. During mirrored readout, the region of active pixels used to generate the Y-flip mirrored image is offset by 1 upper row in horizontal direction so that the readout always starts on the same color pixel.

Figure 17. VGA X/Y-flip image

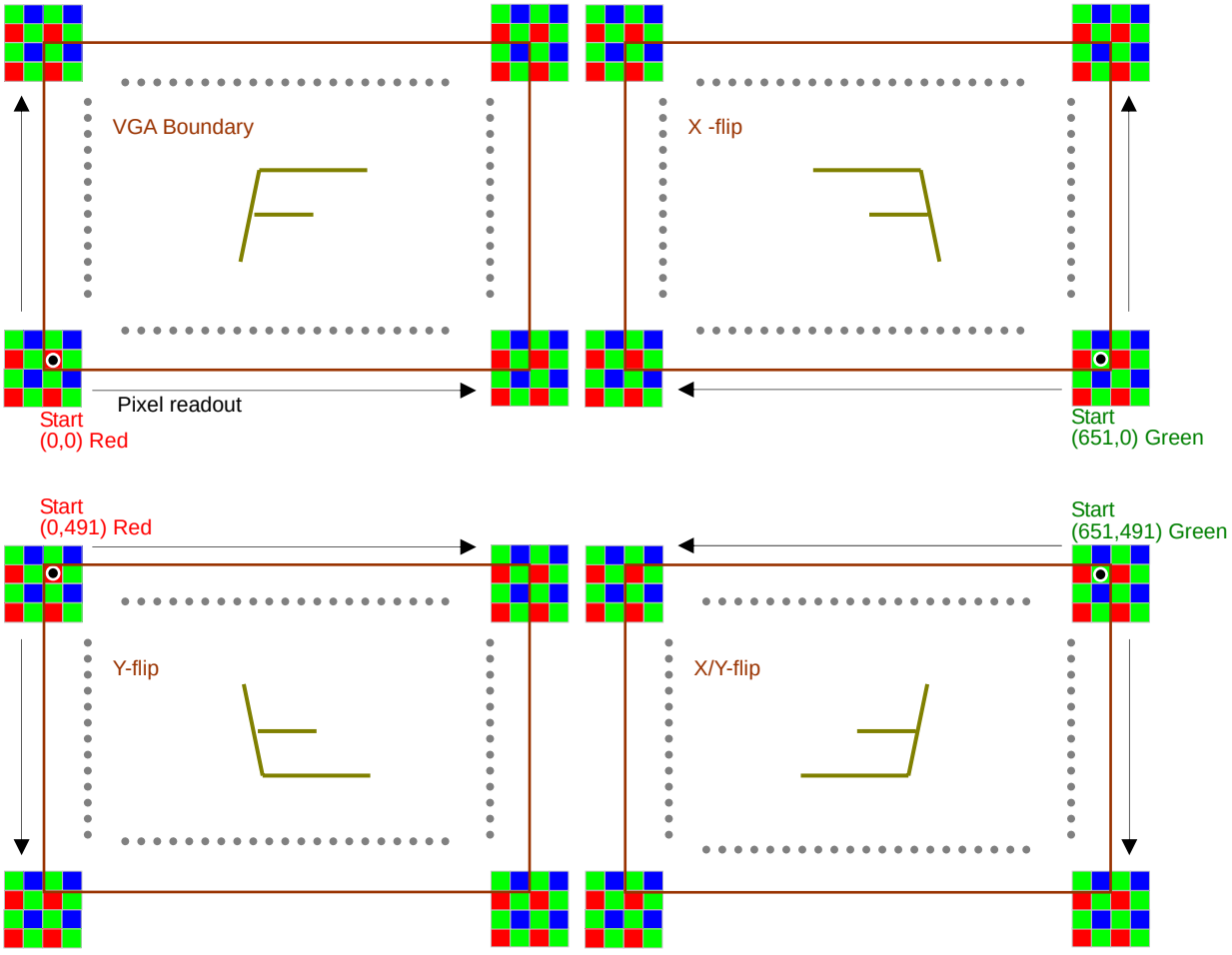


Table 11. VGA start pixel coordinates

Status	Starting pixel coordinates	Starting color	Remark
Original	(0,0)	Red	

X-flip	(651,0)	Green	
Y-flip	(0,491)	Red	
X/Y-flip	(651,491)	Green	

9.4. Analog Gain

The analog gain can either be programmed by the user or controlled by the internal automatic gain control circuit. Raw R, G, B Bayer data are amplified to compensate the analog output levels by the AGAIN factor.

The effective gain follows the herebelow equation.

> Effective gain level=CGAINxFGAIN

=(1+3xCGAIN[1])x(1+CGAIN[0])x(1+FGAIN[4:0]/32)

> CGAIN=(1+3xCGAIN[1])x(1+CGAIN[0])

> FGAIN=1+FGAIN[4:0]/32

Table 12. CGAIN output

CGAIN[1:0]		CGAIN output
D1	D0	
0	0	x1
0	1	x2
1	0	x4
1	1	x8

Figure 18. CGAIN graph

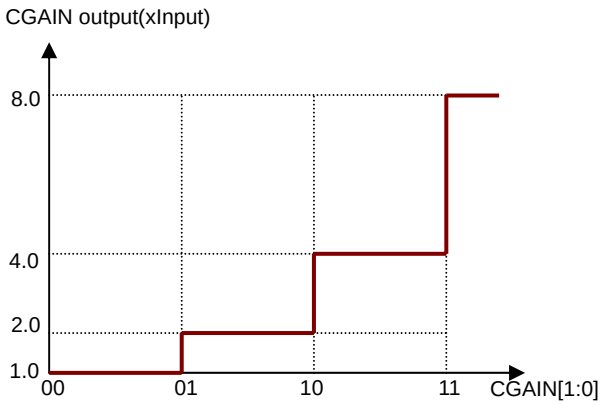


Table 13. FGAIN output

FGAIN[4:0]					FGAIN output
D4	D3	D2	D1	D0	
0	0	0	0	0	1.00
0	1	0	0	0	1.25
1	0	0	0	0	1.50
1	1	0	0	0	1.75
1	1	1	1	1	1.97

Figure 19. FGAIN graph

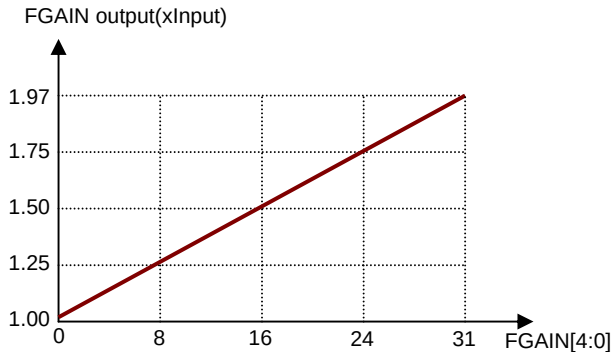
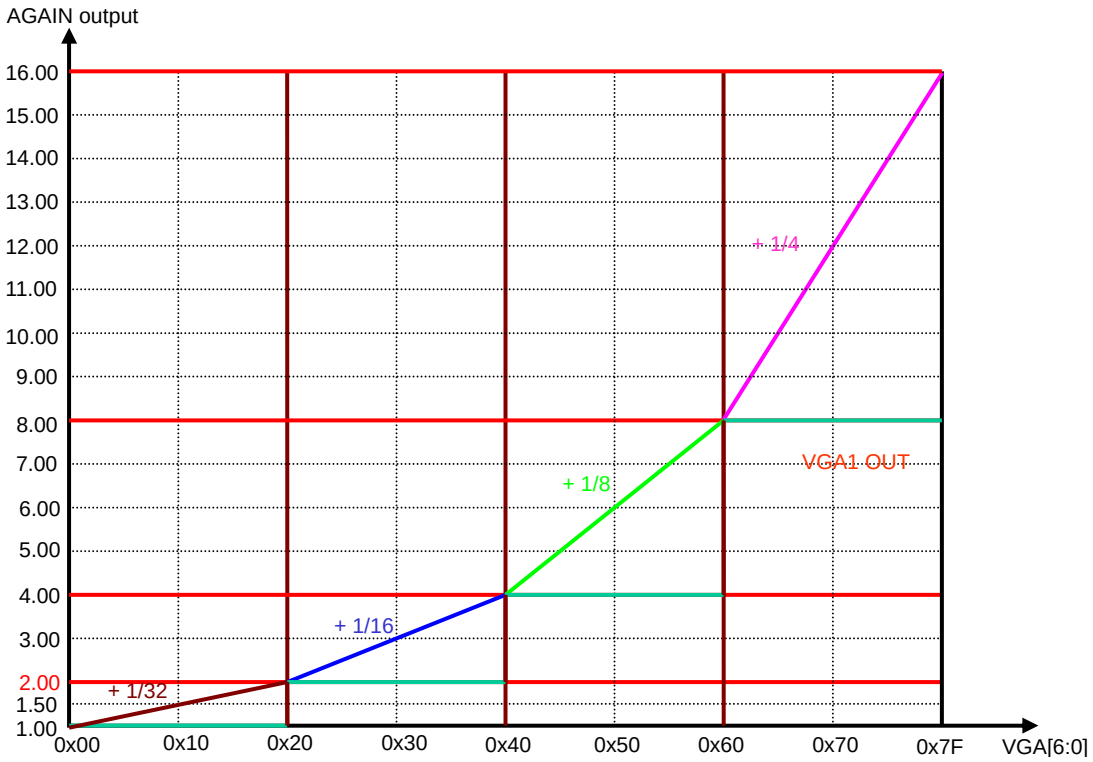


Figure 20. AGAIN output



The AGAIN value automatically varies with the pixel integration time when the auto exposure function works upon the luminance level of the incident light source, and its range is programmed by setting 4 registers, GRANGT, GRANGN, GRANGB, GRANGU. The auto exposure function asserts the AGAIN value between the GRANGB and GRANGN values under the normal brightness condition, and the GRANGN and GRANGT values under low brightness condition. Therefore, these registers are programmed with relation to the equation, GRANGT>=GRANGN >=GRANGB. The GRANGU value Indicates the gain top level if shutter step is less than the STSTN/STSTP.

The manual changes of the gain values may possibly cause to lose image quality, so vendor-recommended register values are highly preferable.

9.5. Color Space Conversion

The chip outputs RGB Bayer and YCbCr data by asserting the function which converts RGB color space to YCbCr. The equation from CCIR-601 is normally used for color space conversion and reverse conversion.

9.6. Color Matrix

In general, the color specifications of the image sensor differ from the fabrication process like color filter, design or something. The color matrix adjusts these unsuitable color specifications unlike the actual color of the subject.

The color matrix of the chip is designed to work deeply interconnected to the color space conversion. Thereby, the user surely takes its mutual relation into consideration to tune the color matrix.

The color matrix & color space conversion use 3x3 color correction matrix shown below.

(R_{out}=Cr, G_{out}=Y, B_{out}=Cb)

$$\begin{pmatrix} R_{out} \\ G_{out} \\ B_{out} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{pmatrix} \times \begin{pmatrix} R_{in} \\ G_{in} \\ B_{in} \end{pmatrix}$$

This chip supports two different methods to get black and white image. The first method to get black and white image is to writing 0x00 in CCMX11, CCMX12, CCMX13, CCMX31, CCMX32 and CCMX33 registers with YCbCr 4:2:2 output format. These 6 registers relate with red and blue color output in color correction matrix. The second method to get black and white image is using OUTCOL[0] register. But please take notice the second method is not YCbCr422 but monochrome 8bit data output format.

9.7. Color Interpolation

Each color Bayer pixel from the image sensor is converted into a R, G, B pixel and the missing color information of a Bayer pixel can be derived from average value of adjacent pixels. 5x5 interpolation window will be shifted by one pixel horizontally and vertically.

9.8. Gamma Correction

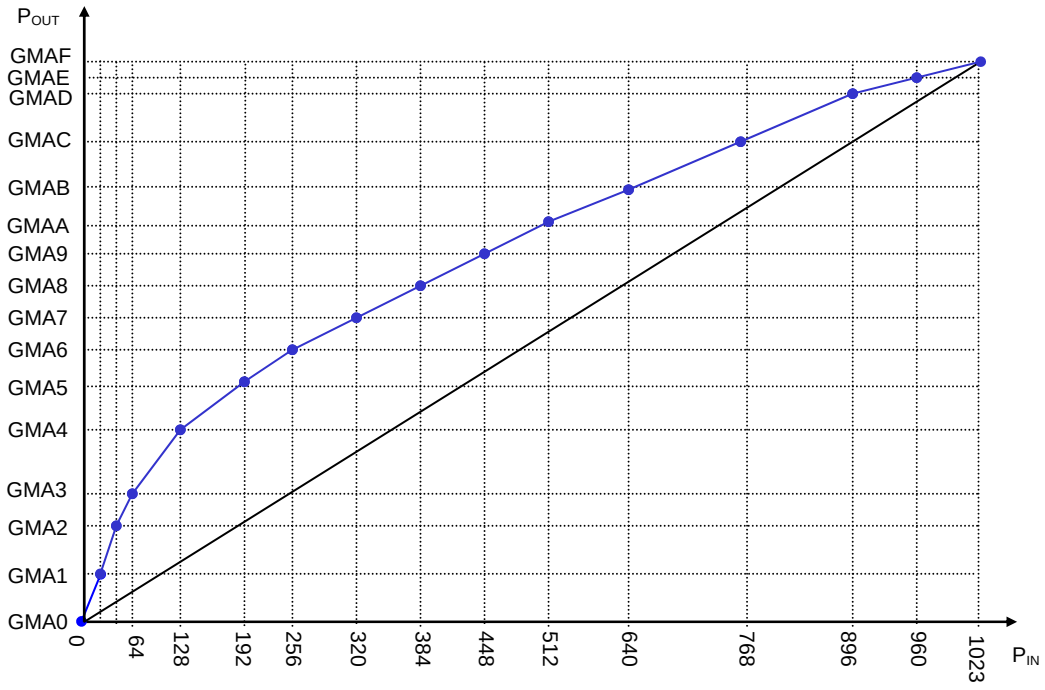
Gamma correction operates on R, G, B pixels respectively to improve non-linear relation between the video signal and the display device output. Piecewise linear method is implemented. 16 piece linear segments are supported and user-programmable.

Table 14. Related registers

Register	Address	Value	Description
GMA0	0xC0	0x00	Gamma point at 0
GMA1	0xC1	0x08	Gamma point at 16
GMA2	0xC2	0x10	Gamma point at 32
GMA3	0xC3	0x1B	Gamma point at 64
GMA4	0xC4	0x37	Gamma point at 128
GMA5	0xC5	0x4D	Gamma point at 192
GMA6	0xC6	0x60	Gamma point at 256
GMA7	0xC7	0x72	Gamma point at 320
GMA8	0xC8	0x82	Gamma point at 384
GMA9	0xC9	0x91	Gamma point at 448
GMAA	0xCA	0xA0	Gamma point at 512

GMAB	0xCB	0xBA	Gamma point at 640
GMAC	0xCC	0xD3	Gamma point at 768
GMAD	0xCD	0xEA	Gamma point at 896
GMAE	0xCE	0xF5	Gamma point at 960
GMAF	0xEF	0xFF	Gamma point at 1023

Figure 21. Gamma graph



9.9. Lens Shading Correction

The circumstance area of pixel array does not have enough quantity of light due to optical characteristics of lens. It causes reduction of signal near peripheral of pixel array. The reduction of signal depends on both of pixel location and color. To compensate the problem, shading correction is done by controlling the gain accordingly to pixel location and color.

9.10. Automatic Flicker Cancellation

Banding noise may be caused when the sensor integration time is not an integer multiple of the

period of light intensity like the environment under a 60/50MHz fluorescent lamp. The flicker is detected using a dedicated algorithm and automatically corrected by adjusted integration time in accordance with frequency of light source for automatic flicker cancellation.

The related registers are TR5A, TR5B, TR5C, TR5D. It is not easy to understand that detail description of automatic Flicker detection and adjustment algorithm. So, please do using reference registers value which recommend SET's.

9.11. Automatic Exposure (AE) Control

AE control algorithm tracks the change of the luminance of a frame image compared frame to frame, and compares calculated luminous to the AE target value. The image brightness is adjusted by controlling analog and digital gains and Shutter time of the pixel array. Luminous integrator filter makes stable image from fast luminous change environment. Also, SIV100B AE algorithm has fast speed control that abnormal luminous change. With AGC(Analog Gain Control) and Shutter Control, SIV100B AE algorithm makes good image which smooth and fast luminous control.

Related Registers are LFCT, LTLV, LRANGE, GMORE, GRANGT/N/B/U, TR48 ~ TR4F and TR50.

SET hope to recommend these registers value for more convenient using.

9.12. Automatic White Balance (AWB) Control

In general, light source have unique color temperature, which may distort the original color of the subject image input into the sensor. The AWB algorithm tracks the white color using the white pixel detection algorithm, and controls the AWB color gain (RGAIN, BGAIN). SIV100B have some registers for the white pixel detection. White pixel is separated from normal pixel of a frame using several registers that are AWBSNGR, AWBSNGB, AWBSNGC, AWBLTO, AWBLBO, AWBWTO and AWBWBO. New generated white position value is compared user target value defined at IHCNTR and IHCNTB. New AWB Gains are generated by the compared results.

There are some registers to support gain range for AWB operation with limited color temperature range that are DGBNDRT, DGBNDRB, DGBNDBT and DGBNDB registers. General operation control option are built in CBFC register, like algorithm selector, windows selector and speed control function. Other control option and test function are defined at TR71, TR72, TR73 and TR74 registers.

SET hope to recommend AWB registers value for more convenient using.

10. Electrical Characteristics

10.1. AC Characteristics

Figure 22. I2C timing

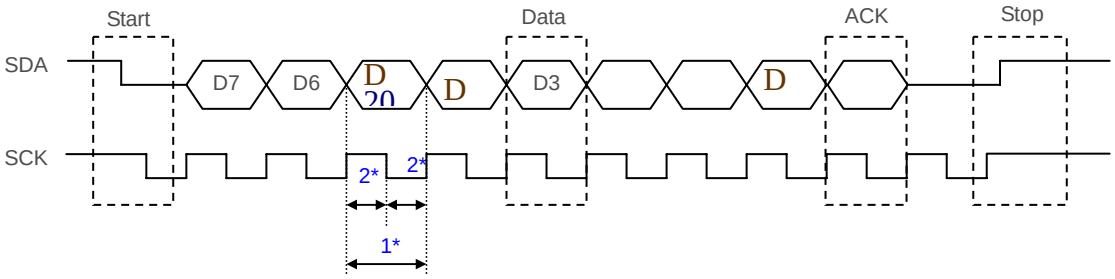


Figure 23. Start Timing

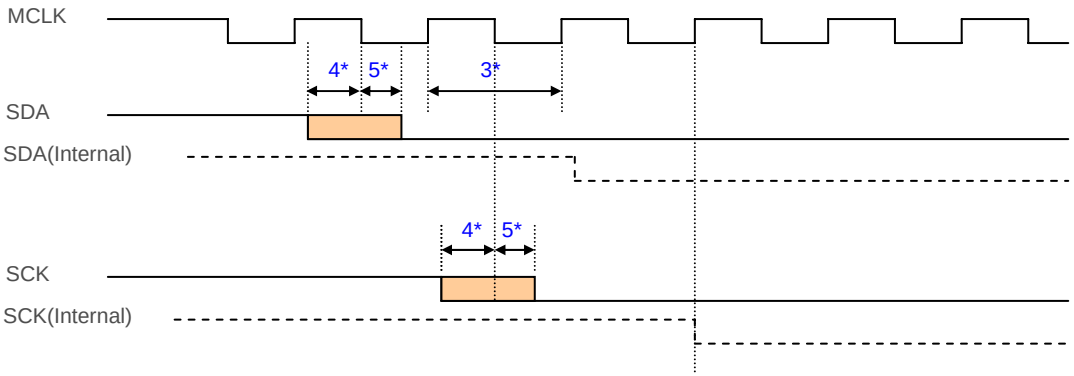


Figure 24. Data timing

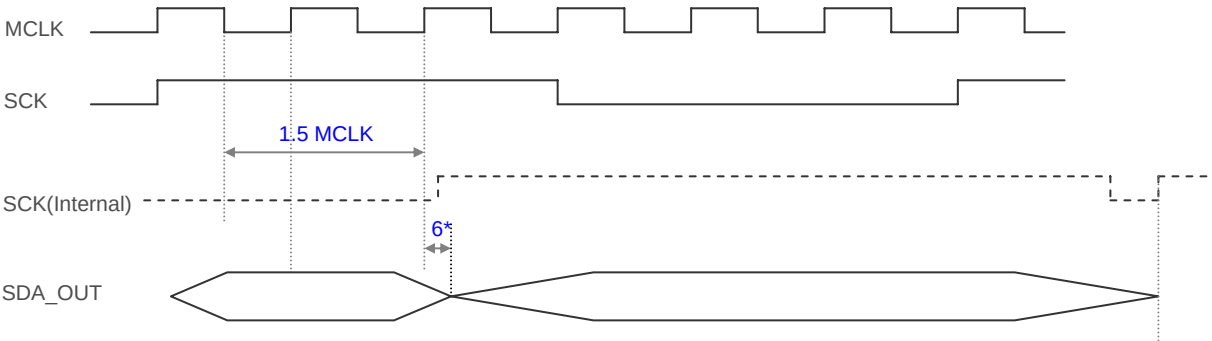


Figure 25. Acknowledge timing

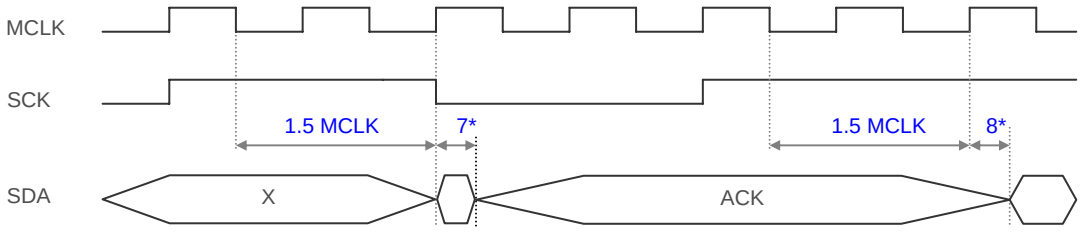


Figure 26. Stop timing

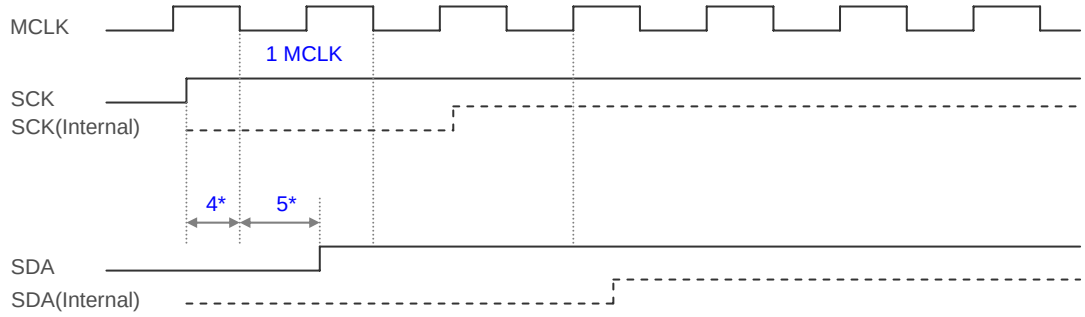
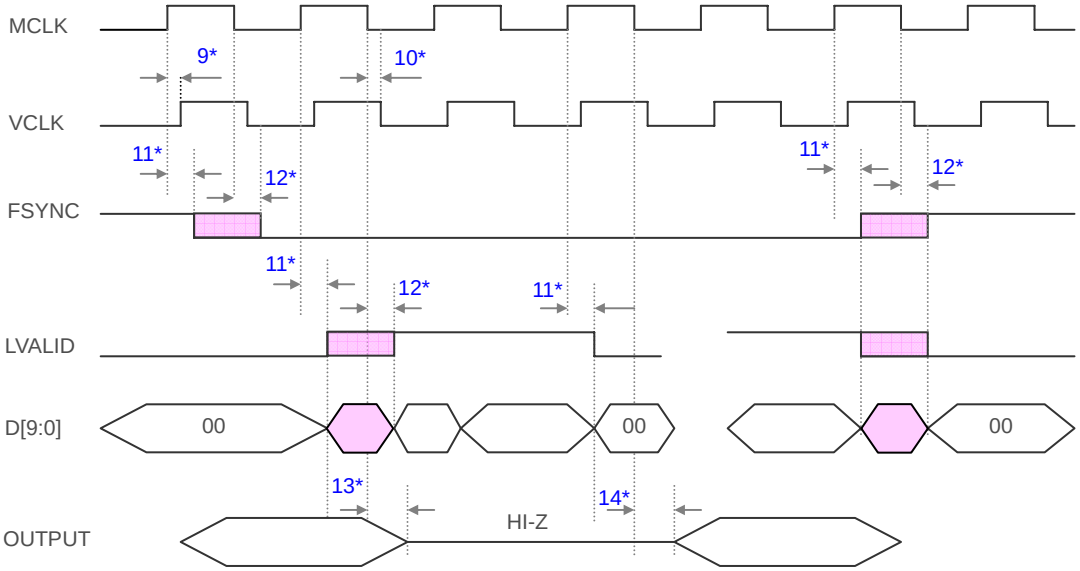


Figure 27. Data output timing



(OUTPUT : PCLK,FSYNC,LVALID,D[7:0])

Table 15. AC Timing Table

Parameter	Symbol	Min	Typical	Max	Unit
SCK,SDA width	1*	4		-	MCLK
SCK Pulse Width	2*	2		-	MCLK
MCLK Period	3*	42(24)	-	-	ns(MHz)
SDA,SCK Data Setup Time	4*	0	-	-	ns
SDA,SCK Data Hold Time	5*	2	2	-	-
MCLK to SDA Out Delay Time	6*	-	-	TBD	ns
MCLK to ACK Valid Time	7*		-	TBD	ns
MCLK to ACK Disable Time	8*		-	TBD	ns
MCLK to VCLK Rising Delay	9*			TBD	ns
MCLK to VCLK Falling Delay	10*			TBD	ns
MCLK(↑) Output Delay	11*			TBD	ns
MCLK(↓) Output Delay	12*			TBD	ns
MCLK to Output HI-Z Delay	13*			TBD	ns
Output Hi-Z to 0/1 Delay	14*			TBD	ns

(Output Loading = 25pf)

10.2. DC Characteristics

10.2.1. Absolute Maximum Ratings

Table 16. Absolute maximum ratings

Symbol	Parameter	Rating	Unit
V_{VDDO}	DC supply voltage for I/O	-0.3 to 3.8	V
V_{VDDC}	DC supply voltage for core	-0.3 to 2.5	V
V_{VDDA}	AC supply voltage for analog	-0.3 to 3.8	V
V_{IN}	DC input voltage	-0.3 to 3.8	V
T_{OPP}	Operating temperature(Performance guaranteed)	-20 to +50	℃
T_{OPF}	Operating temperature(Chip function guaranteed)	-20 to +60	℃
T_{STG}	Storage temperature	-30 to +85	℃

*Note that the image quality even within the operation temperature can be getting worse under the

brightness condition lower than 100 lux.

10.2.2. DC Operating Conditions

Table 17. DC operating conditions

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
V_{VDDO}	DC supply voltage for I/O		1.8	-	2.9	V
V_{VDDC}	DC supply voltage for core		1.6	1.8	2.0	V
V_{VDDA}	AC supply voltage for analog		2.4	2.8	2.9	V
V_{IH}	Input high voltage	CMOS	0.7VDD			V
V_{IL}	Input low voltage				0.3VDD	V
V_{OH}	Output high voltage	I_{OH}=4mA	1.7			V
V_{OL}	Output low voltage	I_{OL}=4mA			0.4	V
I_{IH}	Input leakage current	V_{IN}=VDD			1	uA
I_{IHPU}	Input leakage current with PU	V_{IN} =VDD		37		uA
I_{IL}	Input leakage current	V_{IN} = GND			1	uA
I_{OZ}	3-state output leakage current				1	uA
P_{AVG}	Power dissipation	VDD=2.5V		TBD		mW
P_{STBY}	Stand-by current				TBD	uA

*Note that the VDDO, VDDC, VDDA beyond the limits of hereabove spec can make the image quality deteriorated.

11. Register Description

11.1. Register List

Table 18. Accessible register list

Address (Hex)	Register	Description with Function	Default (Hex)	R/W
01	ChipID	Chip Device ID	0C	R
02	INFO	Device Version	11	R
03	CNTR_A	Sensor Control Register A	04	R/W
04	CNTR_B	Sensor Control Register B	00	R/W
05	CNTR_C	Video Mode Control Register	07	R/W
10	TR10	Reserved		
11	TR11	Reserved		
12	TR12	Reserved		
13	TR13	Reserved		
14	TR14	Reserved		
16	TR16	Reserved		
17	TR17	Reserved		
18	TR18	Reserved		
19	TR19	Reserved		
1A	TR1A	Reserved		
1B	TR1B	Reserved		
1C	TR1C	Reserved		
1D	TR1D	Reserved		
1E	TR1E	Reserved		
1F	TR1F	Reserved		
20	BNKT60	Frame Control Register	00	R/W
21	HBNKT60	Frame Control Register	00	R/W
22	VBNKT60	Frame Control Register	03	R/W
23	BNKT50	Frame Control Register	00	R/W
24	HBNKT50	Frame Control Register	00	R/W
25	VBNKT50	Frame Control Register	67	R/W
30/31	SHTH/SHTL	Shutter Time High/Low Byte	01/F4	R/W

32	AGAIN	Analog Gain Register	10	R/W
33	FRCNT	Frame Rate Counter	0C	R/W
34	STSTN	Preview Mode Anti-Banding Step @ NTSC	7D	R/W

Address (Hex)	Register	Description with Function	Default (Hex)	R/W
35	STSTP	Preview Mode Anti-Banding Step @PAL	96	R/W
36	STSTNF	Anti-Banding NTSC Step	7D	R/W
37	STSTPF	Anti-Banding PAL Step	96	R/W
40	LFCT	Luminous Function Control	A4	R/W
41	LTLV	Luminous Target Level Register	80	R/W
42	LRANG	Luminous Level Checker	77	R/W
43	GMORE	Dark Condition Gain Checker	C8	R/W
44	GRANGT	Luminous Gain Top Selector	4F	R/W
45	GRANGN	Luminous Gain Top Selector	2C	R/W
46	GRANGB	Luminous Gain Top Selector	11	R/W
47	GRANGU	Luminous Gain Top Selector	25	R/W
48	TR48	Reserved		
49	TR49	Reserved		
4A	TR4A	Reserved		
4B	TR4B	Reserved		
4C	TR4C	Reserved		
4D	TR4D	Reserved		
4E	TR4E	Reserved		
4F	TR4F	Reserved		
50	TR50	Reserved		
51	TR51	Reserved		
52	TR52	Reserved		
53	TR53	Reserved		
5A	TR5A	Reserved		
5B	TR5B	Reserved		
5C	TR5C	Reserved		
5D	TR5D	Reserved		
60	AWBCNTR1	Color Balance Function Control	C8	R/W
61	AWBCNTR2	Color Balance Mode Control	8E	R/W

62	AWBLRNG	Color Balance Lock Range Control	01	R/W
63	CRTARGET	Image Hue Red Control	80	R/W
64	CBTARGET	Image Hue Blue Control	80	R/W
65	DGBNDRT	AWB RGAIN Top	DF	R/W
66	DGBNDRB	AWB RGAIN Bottom	70	R/W
67	DGBNDBT	AWB BGAIN Top	DF	R/W
68	DGBNDBB	AWB BGAIN Bottom	78	R/W
69	AWBWHTRT	Single Color Cr Top Value	90	R/W
6A	AWBWHTRB	Single Color Cr Bottom Value	70	R/W
6B	AWBWHTBT	Single Color CB Top Value	90	R/W
6C	AWBWHTBB	Single Color CB Bottom Value	70	R/W
6D	AWBWHTCT	Cr,CB Summation Top Value	84	R/W
6E	AWBWHTCB	Cr,CB Summation Bottom Value	7B	R/W
6F	AWBURNG	AWB Average Mode Lock/Unlock Value	84	R/W
70	AWBLTO	AWB Luminous top	D8	R/W
71	AWBLBO	AWB Luminous Bottom	70	R/W
72	WHTCNTN	White Pixel Count	05	R/W

Address (Hex)	Register	Description with Function	Default (Hex)	R/W
73	WHTCNTL	White Pixel Count for Window Mode	30	R/W
74	AWBGRNG	AWB R Range	07	R/W
75	NEEDEN	Shutter Time for Need Enable	32	R/W
76	NEEDDS	Shutter Time for Need Disable	32	R/W
77	AWBRTO	AWB R gain during AWB Need	B0	R/W
78	AWBBTO	AWB B gain during AWB Need	B5	R/W
7A	RGAIN	AWB Color Balance R-Gain Register	B0	R/W
7B	BGAIN	AWB Color Balance B-Gain Register	B5	R/W
7C	GGAIN	AWB Color Balance G-Gain Register	80	R/W
7F	TR7F	Reserved		
80	IPFUN	IDP Function Control	AE	R/W
81	SIGCNT	Signal Output Control	1D	R/W
82	OUTFMT	Output Format Control	D5	R/W
83	TR83	Reserved		
84	ISPOPT	ISP Option Register	FF	R/W

85	VBTC	Vertical Blank Time Control	00	R/W
86	DCTRL	DPC Control	E0	R/W
87	NTHLD	Defect Threshold	10	R/W
88	DSTRT	DPC Change Start Gain	20	R/W
89	DSLOP	DPC Change Gain Slope	04	R/W
8A	RxPGA	R Pixel Pre Gain	80	R/W
8B	GrPGA	G1(GR-Line) Pixel Pre Gain	80	R/W
8C	GbPGA	G2(GB-Line) Pixel Pre Gain	80	R/W
8D	BxPGA	B Pixel Pre Gain	80	R/W
8E	ROFST	Red Pixel Offset	00	R/W
8F	G1OFST	G1(GR-Line) Pixel Offset	00	R/W
90	G2OFST	G2(GB-Line) Pixel Offset	00	R/W
91	BOFST	Blue Pixel Offset	00	R/W
92	FILCNT	Filter Control	FE	R/W
93	GLPFTH	Gr,Gb LPF Threshold Value	00	R/W
94	GLPFSLOP	Gr,Gb LPF Slop Gain	00	R/W

Address (Hex)	Register	Description with Function	Default (Hex)	R/W
95	GLPFEND	Gr,Gb LPF End Value	FF	R/W
96	CLPFTH	R,B LPF Threshold Value	00	R/W
97	CLPFSLOP	R,B LPF Slop Gain	00	R/W
98	CLPFEND	R,B LPF End Value	FF	R/W
99	LPFSTRT	LPF Start Gain	20	R/W
9A	GLEVEL	LPF Up & Down Select Level	00	R/W
9B	BLCFUN	BLC Function Register	00	R/W
9C	RxBLCL	Red Pixel Dark Value	10	R/W
9D	GrBLCL	Green(GR-Line) Pixel Dark Value	10	R/W
9E	GbBLCL	Green(GB-Line) Pixel Dark Value	10	R/W
9F	BxBLCL	Blue Pixel Dark Value	10	R/W
A0	RxFBLC	Red Pixel Fixed Dark Value	10	R/W
A1	GrFBLC	G1(GR-Line) Pixel Fixed Dark Value	10	R/W
A2	GbFBLC	G2(GB-Line) Pixel Fixed Dark Value	10	R/W
A3	BxFBLC	Blue Pixel Fixed Dark Value	10	R/W

A4	SPOSIA	Shading Area Gain A	FD	R/W
A5	SPOSIB	Shading Area Gain B	CB	R/W
A6	SPOSIC	Shading Area Gain C	A8	R/W
A7	SPOSID	Shading Area Gain D	64	R/W
A8	SPOSIE	Shading Area Gain E	21	R/W
A9	SHDHORR	Red Pixel X-axis Shading Gain	00	R/W
AA	SHDVERR	Red Pixel Y-axis Shading Gain	00	R/W
AB	SHDHORG	Green Pixel X-axis Shading Gain	00	R/W
AC	SHDVERG	Green Pixel Y-axis Shading Gain	00	R/W
AD	SHDHORB	Blue Pixel X-axis Shading Gain	00	R/W
AE	SHDVERB	Blue Pixel Y-axis Shading Gain	00	R/W
AF	SHDCNTX	X-axis Shading Center Position	A1	R/W
B0	SHDCNTY	Y-axis Shading Center Position	81	R/W

Address (Hex)	Register	Description with Function	Default (Hex)	R/W
B1	GMA0	Gamma Point 0	00	R/W
B2	GMA1	Gamma Point 1	08	R/W
B3	GMA2	Gamma Point 2	10	R/W
B4	GMA3	Gamma Point 3	1B	R/W
B5	GMA4	Gamma Point 4	37	R/W
B6	GMA5	Gamma Point 5	4D	R/W
B7	GMA6	Gamma Point 6	60	R/W
B8	GMA7	Gamma Point 7	72	R/W
B9	GMA8	Gamma Point 8	82	R/W
BA	GMA9	Gamma Point 9	91	R/W
BB	GMAA	Gamma Point A	A0	R/W
BC	GMAB	Gamma Point B	BA	R/W
BD	GMAC	Gamma Point C	D3	R/W
BE	GMAD	Gamma Point D	EA	R/W
BF	GMAE	Gamma Point E	F5	R/W
C0	GMAF	Gamma Point F	FF	R/W
C1	CMA11	Color Matrix Coefficient 11	3B	R/W
C2	CMA12	Color Matrix Coefficient 12	CE	R/W
C3	CMA13	Color Matrix Coefficient 13	F7	R/W

C4	CMA21	Color Matrix Coefficient 21	13	R/W
C5	CMA22	Color Matrix Coefficient 22	25	R/W
C6	CMA23	Color Matrix Coefficient 23	07	R/W
C7	CMA31	Color Matrix Coefficient 31	F2	R/W
C8	CMA32	Color Matrix Coefficient 32	C7	R/W
C9	CMA33	Color Matrix Coefficient 33	47	R/W
CA	ECTRL	Sharpness Control	80	R/W
CB	EUGAIN	Edge Upper Gain	20	R/W
CC	EDGAIN	Edge Down Gain	40	R/W
CD	EUCORE	Edge Upper Core Value	04	R/W
CE	EDCORE	Edge Down Core Value	04	R/W
CF	EUCLIP	Edge Upper Clip Value	20	R/W
D0	EDCLIP	Edge Down Clip Value	20	R/W
D1	ESTART	Edge Suppress Start Gain	20	R/W
D2	ESLOP	Edge Suppress Slope	10	R/W
D3	EDGLEVEL	Edge Threshold Level	00	R/W

Address (Hex)	Register	Description with Function	Default (Hex)	R/W
D4	YGAIN	Contrast Stretch Gain	10	R/W
D5	CRGAIN	Cr Color Saturation Gain	10	R/W
D6	CBGAIN	Cb Color Saturation Gain	10	R/W
D7	BRTCNT	Brightness Control	00	R/W
D8	IEFCT	Image Effect Control	00	R/W
D9	EFCB	Cb Value for Image Effect	60	R/W
DA	EFCR	Cr Value for Image Effect	A0	R/W
DB	YTOP	Luminance Top Clip Value	FF	R/W
DC	YBOT	Luminance Bottom Clip Value	10	R/W
DD	CRTOP	Cr Top Clip Value	FF	R/W
DE	CRBOT	Cr Bottom Clip Value	00	R/W
DF	CBTOP	Cb Top Clip Value	FF	R/W
E0	CBBOT	Cb Bottom Clip Value	00	R/W
E1	GSTRT	Color Saturation Suppression Start Gain	30	R/W
E2	GSLOP	Color Saturation Suppression Slope	88	R/W
E3	TRE3	Reserved		

E4	TRE4	Reserved		
E5	TRE5	Reserved		
E6	TRE6	Reserved		
F0	WDATH	Window Data High Byte	34	R/W
F1	WHSRTL	Window Horizontal Start Low Byte	00	R/W
F2	WHWIDL	Window Horizontal Width Low Byte	FF	R/W
F3	WVSRTL	Window Vertical Start Low Byte	00	R/W
F4	WVWIDL	Window Vertical Width Low Byte	FF	R/W

The registers unsaid herein are vendor-reserved, and they can cause critical troubles in chip performance arising from the abnormal uses. SET could release the additional application note for further technical supports to fine-tune the chip accordingly to each application use. Please contact SET for further information if necessary.

11.2. Accessible Register Feature

ChipID [R]

Chip Device ID **Address [01h], Default [0Ch]**

INFO [R]

Device Version **Address [02h], Default [11h]**

CNTR_A [R/W]

Sensor Control Register A **Address [03h], Default [04h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VDRV_SEL1	VDRV_SEL0	ODRV_SEL1	ODRV_SEL0	-	OPAD_EN	PWDN	SNR_EN
Default	0	0	0	0	0	1	0	0

Bit[7:6] VDRV_SEL[1:0] : Select an drive capability for VCLK output

00 Output drive capability = 4mA

01 Output drive capability = 8mA

00 Output drive capability = 12mA

00 Output drive capability = 16mA

Bit[5:4] ODRV_SEL[1:0] : Select an drive capability for other outputs

Bit[2] OPAD_EN : It activates an output pin operation. Its value should be '1' to afford a sensor output. In case of '0', all of output pins get disabled.

0 All output pads are in HI_Z state(Except SDA)

1 Normal operation mode

Bit[1] PWDN : Control a power-down mode

If the power down mode function comes into 'enable', every block operation of the chip except I2C stops to consume the lowest power. In such a case, the SNR_EN value can be negligible because the power down function is prior to all other bits of the CNTR_A register.

0 Normal operation mode

1 Power-down mode

Bit[0] SNR_EN : Assert the device into an idle or dynamic mode.

In the idle mode when the SNR_EN function goes disabled, its internal clock also stays disabled.

0 Disable image output(Idle mode)

1 Enable image output(Dynamic mode)

CNTR_B [R/W]

Sensor Control Register B **Address [04h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	-	-	-	-	CLK_DIV		Y_FLIP	X_FLIP
Default	0	0	0	0	0	0	0	0

Bit[3:2] CLK_DIV : Clock divider control

This function, whose values are internal clock frequency control bits, can afford a clock divider and define a divider rate.

* Refer to the description, 'Relation of Clocks'.

Bit[1] Y_FLIP : Control vertical flip image

0 Normal image

1 Vertical flip image

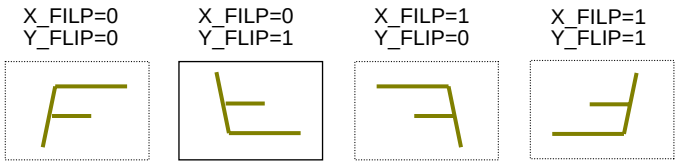
Bit[0] X_FLIP : Control horizontal flip image

0 Normal image

1 Horizontal flip image

* Refer to the description, 'X/Y-Flip image and data readout order'.

Figure 28. X/Y flip image accordingly to register setting



CNTR_C [R/W]

Video Mode Control Register **Address [05h], Default [07h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	-	-	-	-	-	VMODE		

Default	x	x	x	x	x	1	1	1

The user variable window modes are applicable by setting the WINEN function of the OUTFMT[3]. Once enabled, the output format and window sizes can be redefined by programming these registers.

* Refer to the detailed description, 'Video Output Size Information'

BNKT60 [R/W]

Frame Control Register **Address [20h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	-	-	HBNKT60		-	-	VBNKT60	
Default	0	0	0	0	0	0	0	0

> Horizontal Blank Time : HBNKT60[9:0] = {BNKT60[5:4], HBNKT60[7:0]}

> Vertical Blank Time : VBNKT60[9:0] = {BNKT60[1:0], VBNKT60[7:0]}

> 1 Row Time = (Display Width + HST(155) + Horizontal Blank Time + 1) x PCLK

HBNKT60 [R/W]

Frame Control Register **Address [21h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	HBNKT60							
Default	0	0	0	0	0	0	0	0

Unit : PCLK(1/2 MCLK)

VBNKT60 [R/W]

Frame Control Register **Address [22h], Default [03h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VBNKT60							
Default	0	0	0	0	0	0	1	1

Unit : Row

BNKT50 [R/W]

Frame Control Register **Address [23h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	-	-	HBNKT50		-	-	VBNKH50	
Default	0	0	0	0	0	0	0	0

> Horizontal Blank Time : HBNKT50[11:0] = {BNKT50[5:4], HBNKT50[7:0]}

> Vertical Blank Time : VBNKT50[11:0] = {BNKT50[1:0], VBNKT50[7:0]}

> 1 Row Time = (Display Width + HST(155) + Horizontal Blank Time + 1) x PCLK

HBNKT50 [R/W]

Frame Control Register **Address [24h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	HBNKT50							
Default	0	0	0	0	0	0	0	0

Unit : PCLK(1/2 MCLK)

VBNKT50 [R/W]

Frame Control Register **Address [25h], Default [67h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VBNKT50							
Default	0	1	1	0	0	1	1	1

Unit : Row

SHTH/SHTL [R/W]

Frame Control Register **Address [30h/31h], Default [01h/F4h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SHTH/SHTL							
Default	x	x	x	x	x	x	x	x

Integration time is calculated by line unit.

AGAIN [R/W]

Analog Gain Register **Address [32h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED	CGAIN		FGAIN				
Default	0	0	0	1	0	0	0	0

This register controls an analog gain level. Each CGAIN(Coarse Gain) and FGAIN(Fine Gain) functions make analog gain levels variously controllable.

If the AEFUN function of the LFCT[7] register is set disabled, the AGAIN register value defines the analog gain level as follows.

* Refer to the description, 'Analog Gain'.

Once the AEFUN function gets enabled, the AE algorithm automatically controls the analog gain level.

FRCNT [R/W]

Frame Rate Counter **Address [33h], Default [0Ch]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED	RESERVED	FRCNT					
Default	-	-	0	0	1	1	0	0

The FRCNT register defines the maximum exposure time of the auto exposure function by writing the integer proportion of the STSTN/STSTP.

> The Maximum Exposure Time = STSTN (or STSTP) Time x FRCNT.

By this, the minimum frame rate is defined. The default value(8'h0C) of the FRCNT register has the minimum frame rate as follows.

> AC60Hz Maximum Exposure time = STSTN Time x FRCTRL = 1/120 sec x 12 = 0.100 sec = 10 fps

> AC50Hz Maximum Exposure time = STSTP Time x FRCTRL = 1/100 sec x 12 = 0.120 sec = 8.3 fps

STSTN [R/W]

Anti-banding Step at the NTSC Mode **Address [34h], Default [7Dh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	STSTN							
Default	0	1	1	1	1	1	0	1

The anti-banding step at the NTSC mode.

Unit : 120Hz line

STSTP [R/W]

Anti-banding Step at the PAL Mode **Address [35h], Default [96h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	STSTP							
Default	1	0	0	1	0	1	1	0

The anti-banding step at the PAL mode.

Unit : 100Hz line

STSTNF [R/W]

Anti-banding NTSC Step at the PAL Mode **Address [36h], Default [7Dh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	STSTNF							
Default	0	1	1	1	1	1	0	1

120Hz lines at the PAL mode

STSTPF [R/W]

Anti-banding PAL Step at the NTSC Mode **Address [37h], Default [96h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	STSTPF							
Default	1	0	0	1	0	1	1	0

100Hz lines at the NTSC mode

LFCT [R/W]

Luminous Function Control **Address [40h], Default [A4h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AEFUN	AEWIN	AECNT	-	AEMAG	AEBLC	FSEL50	INDOOR
Default	1	0	1	0	0	1	0	0

Bit[7] AEFUN : AE enable

Bit[6] AEWIN : Define the block side of the AE window.

Bit[5] AECNT : Support the AE center mode.

Bit[3] AEMAG : Select the max. value of the BLC-Level

0 max. 'h10

1 max. 'h30

Bit[2] AEBLC : Increase the brightness by decreasing the BLC-Level in dark condition.

Bit[1] FSEL50 : Select 50Hz PAL power, and the STSTP as a shutter step when enabled(1). Programming it disable(0) selects the STSTN step.

Bit[0] INDOOR : Disable the pixel mode. It can't be used at the outdoor bright condition while banding doesn't show up. The anti-flicker mode operation works under the fluorescent light condition when enabled(1).

0 Automatic indoor and outdoor mode

1 Only indoor Mode

LTLV [R/W]

Luminous Target Level **Address [41h], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	LTLV							
Default	1	0	0	0	0	0	0	0

This function settles the luminous target level of the auto exposure function.

LRANG [R/W]

Luminous Level Checker **Address [42h], Default [77h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	LRANGH				LRANGL			
Default	0	1	1	1	0	1	1	1

This register sets a standard value to control the integration time, or gain, with the LRANGH function multiplied by 4, and LRANGL by 2.

The 4xLRANGH value should be always more than the 2xLRANGL value.

GMORE [R/W]

Dark Condition Gain Checker **Address [43h], Default [C8h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GSEL	GAINLEVEL						
Default	1	1	0	0	1	0	0	0

Bit[7] GSEL : Select the analog gain condition that MORETIME is disabled.

0 If the GAINLEVEL is 7, the MORETIME is disabled.

1 If the GAINLEVEL is 15, the MORETIME is disabled.

Bit[6:0] GAINLEVEL : If the analog gain is more than GAINLEVEL, the MORETIME is enabled.

GRANGT/N/B/U [R/W]

Dark Condition Gain Checker **Address [44h/45h/46h/47h], Default [4Fh/2Ch/11h/25h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED	GRANGT/N/B/U						
Default	-	x	x	x	x	X	x	X

Bit[6:0] GRANGT : Indicate the gain top level after the max integration in a dark condition.

GRANGN : Indicate the gain top level if integration time is not the max, and gain bottom level if integration time is the max.

GRANGB : Indicate the gain bottom level if integration time is not the max.

GRANGU : Indicate the gain top level if shutter step is less than the STSTN/STSTP.

AWBCNTR1 [R/W]

AWB Common Control Registers 1 **Address[60h],Default [C8h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBMODE		AWBSEN	CBSCL	AWBRate	AWBOPT		
Default	1	1	0	0	1	0	0	0

Bit[7:6] AWBMODE : AWB Algorithm Selector

00 AWB off

01 Average Mode

02 White Tracking Mode

11 AWB Advanced Mode

Bit[5] AWBSEN : Single Color Detect Enable

Bit[4] CBSCL : AWB gain speed up

Bit[2:0] AWBOPT : This function control the AWB Operation Mode.

000, 001, 101 normal operation

010 Gain move fix at Integration Time < NEEDEN

011 Fix to AWBRTO,AWBBTO at Integration Time < NEEDEN

100 Fix to AWBRTO,AWBBTO

110 DGBNDRB,DGBNDBT Gain Fix

111 DGBNDRT,DGBNDBB Gain Fix

AWBCNTR2 [R/W]

AWB Common Control Registers 2 **Address[61h],Default [8Eh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBLSEL	AWBLOCK		AWBULOCK		AWBAEEN	AWBAE	
Default	1	0	0	0	1	1	1	0

Bit[7] AWBLOCK Selector

0 Using the 'AWBLOCK' for AWB Lock Condition Check

1 Using the 'AWBULOCK' for AWB Lock Condition Check

Bit[6:5] AWBLOCK : AWB Lock Condition Checker

00 AWB Lock Condition1

01 AWB Lock Condition2

10 Condition1 and Condition2

11 Condition1 or Condition2

Bit[4:3] AWBULOCK : AWB Unlock Condition Checker

00 AWB Unlock Condition1

01 AWB Unlock Condition3

10 Condition1 & Condition3

11 Condition1 or Condition3

Bit[2] AWBAEEN : AE related AWB Operation Mode Enable.

Bit[1:0] AWBAE : AE Condition Selector for AWB Operation.

00 AE Condition 0

01 AE Condition 1

10 AE Condition 2

11 AE Condition 3

CBRC [R/W]

Color Balance Lock Range Control **Address [62h], Default [01h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBLRNGD				AWGLTNGC			
Default	0	0	0	0	0	0	0	1

Bit[7:4] AWB Range D

Bit[3:0] AWB Range C

CRTARGET [R/W]

Image Hue Red Control **Address [63h], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CRTARGET							
Default	1	0	0	0	0	0	0	0

AWB Cr target value register

CBTARGET [R/W]

Image Hue Blue Control **Address [64h], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CBTARGET							
Default	1	0	0	0	0	0	0	0

AWB Cb target value register

DGBNDRT [R/W]

AWB RGAIN Top **Address [65h], Default [DFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DGBNDRT							
Default	1	1	0	1	1	1	1	1

AWB RGAIN top indicator

DGBNDRB [R/W]

AWB RGAIN Bottom **Address [66h], Default [70h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0

Function	DGBNDRB							
Default	0	1	1	1	0	0	0	0

AWB RGAIN bottom indicator

DGBNDBT [R/W]

AWB BGAIN Bottom **Address [67h], Default [DFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DGBNDBT							
Default	1	1	0	1	1	1	1	1

AWB BGAIN top indicator

DGBNDBB [R/W]

AWB RGAIN Bottom **Address [68h], Default [78h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DGBNDBB							
Default	0	1	1	1	1	0	0	0

AWB BGAIN bottom indicator

AWBWHTRT [R/W]

Cr White Top Range Definition **Address [69h], Default [90h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBWHTRT							
Default	1	0	0	1	0	0	0	0

AWBWHTRT : AWB White Pixel CR Top Value

AWBWHTRB [R/W]

Cr White Bottom Range Definition **Address [6Ah], Default [70h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBWHTRB							
Default	0	1	1	1	0	0	0	0

AWBWHTRB : AWB White Pixel CR Bottom Value

AWBWHTBT [R/W]

Cb White Top Range Definition **Address [6Bh], Default [90h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBWHTBT							
Default	1	0	0	1	0	0	0	0

AWBWHTBT : AWB White Pixel CB Top Value

AWBWHTBB [R/W]

Cb White Bottom Range Definition **Address [6Ch], Default [70h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBWHTBB							
Default	0	1	1	1	0	0	0	0

AWBWHTBB : AWB White Pixel CB Bottom Value

AWBWHTCT [R/W]

Cb +Cr White Top Range Definition **Address [6Dh], Default [84h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBWHTCT							
Default	1	0	0	0	0	1	0	0

AWBWHTCT : AWB White Pixel CR,CB Average Top Value

AWBWHTCB [R/W]

Cb +Cr White Bottom Range Definition **Address [6Eh], Default [7Bh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBWHTCB							
Default	0	1	1	1	1	0	1	1

AWBWHTCB : AWB White Pixel CR,CB Average Bottom Value

AWBURNG [R/W]

AWB Average Mode Lock/Unlock Range **Address [6Fh], Default [84h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	UNLOCK				LOCK			
Default	1	0	0	0	0	1	0	0

UNLOCK : Average Mode Unlock Value

LOCK : Average Mode Lock Value

AWBLTO [R/W]

AWB Luminous top **Address [70h], Default [D8h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBLTO							
Default	1	1	0	1	1	0	0	0

AWBLTO : White Mode Luminance Top Level

AWBLBO [R/W]

AWB Luminous bottom **Address [71h], Default [70h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBLBO							

Default	0	1	1	1	0	0	0	0

AWBLBO : White Mode Luminance Bottom Level

WHTCNTN [R/W]

White Pixel Count **Address [72h], Default [05h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	Sign	WHTCNTN						
Default	0	0	0	0	0	1	0	1

WHTCNTN : White Mode White Pixel Minimum Count(X32)

WHTCNTL [R/W]

The Minimum White Pixel Counter **Address [73h], Default [30h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	WHTCNTL							
Default	0	0	1	1	0	0	0	0

WHTCNTL : Window Mode Unlock Condition Detect White Pixel Count(X32)

AWBGRNG [R/W]

AWB G Range **Address [74h], Default [07h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBGRNG							
Default	0	0	0	0	0	1	1	1

AWBGRNG : R,B Gain Range for G Gain

NEEDEN [R/W]

Shutter Time for Need Enable **Address [75h], Default [32h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	NEEDEN							
Default	0	0	1	1	0	0	1	0

NEEDEN : Start Integration Time for Bright Condition

NEEDDS [R/W]

Shutter Time for Need disable **Address [76h], Default [32h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	NEEDDS							
Default	0	0	1	1	0	0	1	0

NEEDDS : End Integration Time for Bright Condition

AWBRTO [R/W]

AWB R gain during AWB Need **Address [77h], Default [B0h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBRTO							
Default	1	0	1	1	0	0	0	0

AWBRTO : R Gain for Bright Condition

AWBBTO [R/W]

AWB B gain during AWB Need **Address [78h], Default [B5h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	AWBBTO							
Default	1	0	1	1	0	1	0	1

AWBBTO : B Gain for Bright Condition

RGAIN [R/W]

Color Balance R-Gain Register **Address [7Ah], Default [B0h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RGAIN							
Default	1	0	1	1	0	0	0	0

R Color Balance Gain (1/128 ~ 255/128)

BGAIN [R/W]

Color Balance B-Gain Register **Address [7Bh], Default [B5h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BGAIN							
Default	1	0	1	1	0	1	0	1

B Color Balance Gain (1/128 ~ 255/128)

GGAIN [R/W]

Color Balance G-Gain Register **Address [7Ch], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GGAIN							
Default	1	0	0	0	0	0	0	0

G Color Balance Gain (1/128 ~ 255/128)

IPFUN [R/W]

Image Digital Processing Function Control **Address [80h], Default [AEh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	PGAEN	FIXAWB	DGAEN	FIXBLC	BLCEN	GMAEN	CSCEN	SHDEN
Default	1	0	1	0	1	1	1	0

Bit[7] PGAEN : Pre Offset gain function enable

Bit[6] FIXAWB : AWB gain fix enable

Bit[5] DGAEN : AWB gain function enable

Bit[4] FIXBLC : Black level value fix enable

Bit[3] BLCEN : BLC function enable

Bit[2] GMAEN : Gamma function enable

Bit[1] CSCEN : Color matrix function enable

Bit[0] SHDEN : Shading function enable

SIGCNT [R/W]

Signal Output Control **Address [81h], Default [1Dh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VBTEN	VBLKEN	HBLKEN	OSYNC	LPOL	VPOL	LVLD	PVLD
Default	0	0	0	1	1	1	0	1

Bit[7] VBTEN : Vertical blank time function enable

Bit[6] VBLKEN : FSYNC Enable during VBLANK Time

Bit[5] HBLKEN : HSYNC Enable during VBLANK Time

Bit[4] OSYNC : Y,C,LVALID & FSYNC edge sync control

0 negative edge VCLK

1 positive edge VCLK

Bit[3] LPOL : LVALID polarity control

0 Active low

1 Active high

Bit[2] VPOL : FSYNC polarity control

0 Active low

1 Active high

Bit[1] LVLD : LVALID enable during FSYNC

0 Not active

1 Active

Bit[0] PVLD : VCLK enable during FSYNC & LVALD

0 Not active

1 Active

OUTFMT [R/W]

Output Format Control **Address [82h], Default [D5h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	UVMSEL	RESERVED	YFIRST	UFIRST	WINEN	FORMAT		
Default	1	1	0	1	0	1	0	1

Bit[7] UVMSEL : Cb, Cr mean value selection

0 Not Mean

1 Mean

Bit[5] YFIRST : Y first control

0 C First

1 Y First

Bit[4] UFIRST : C first control

0 Cr First

1 Cb First

Bit[3] WINEN : Window function enable

Bit[2:0] FORMAT : Format selection

000 10-bit bypass Bayer

001 10-bit DPCed Bayer

010 Mono

011 Inverted Mono

101 YCbCr422

IDPOPT [R/W]

IDP Option Register **Address [84h], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DiaDPCEN	DPCEN	INTEN	EDGEN	LPFEN	COLEN	RESERVED	
Default	1	1	1	1	1	1	1	1

Bit[7] DiaDPCEN : Diagonal DPC Select Bit

Bit[6] DPCEN : DPC enable bit

Bit[5] INTEN : Interpolation enable bit

0 Bayer data

1 Interpolation data

Bit[4] EDGEN : Sharpness enable bit

Bit[3] LPFEN : Low pass filter enable bit(sharpness control block)

Bit[2] COLEN : Image control enable bit

VBTC [R/W]

Vertical Blank Time Control **Address [85h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	VLRVAL					BLDVAL		
Default	0	0	0	0	0	0	0	0

Bit[7:3] VLRVAL : VLR cancellation value for FSYNC

Bit[2:0] BLDVAL : BLD cancellation value for FSYNC

DCTRL [R/W]

DPC Control **Address [86h], Default [E0h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DPC1	DPC2	DPC3	DPC4	DPC5	DPC6	DPC7	DPC8
Default	1	1	1	0	0	0	0	0

Bit[7] DPC1 : Highest value change for normal condition

Bit[6] DPC2 : 2nd Highest value change for normal condition

Bit[5] DPC3 : Black blemish compensation for normal condition

Bit[4] DPC4 : Median filter for normal condition

Bit[3] DPC5 : Highest value change for dark condition

Bit[2] DPC6 : 2nd Highest value change for dark condition

Bit[1] DPC7 : Black blemish compensation for dark condition

Bit[0] DPC8 : Median filter for dark condition

DTHLD [R/W]

Defect Threshold **Address [87h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	DTHLD							

Default	0	0	0	1	0	0	0	0

Bit[7:0] DTHLD : DPC threshold value

DSTART [R/W]

DPC Change Start Gain **Address [88h], Default [20h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED	DSTART						
Default	0	0	1	0	0	0	0	0

Bit[6:0] DSTART : DPC start gain

DSLOP [R/W]

DPC Change Gain Slope **Address [89h], Default [04h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED				DSLOP			
Default	0	0	0	0	0	1	0	0

Bit[3:0] DSLOP : DPC SLOP from normal to dark condition

RxPGA [R/W]

Red Pixel Pre Gain **Address [8Ah], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RxPGA							
Default	1	0	0	0	0	0	0	0

Bit[7:0] RxPGA : Red Pixel Pre Gain(/128)

G1PGA [R/W]

G1(GR-Line) Pixel Pre Gain **Address [8Bh], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	G1PGA							
Default	1	0	0	0	0	0	0	0

Bit[7:0] G1PGA : Green(RG-Line) Pixel Pre Gain(/128)

G2PGA [R/W]

G2(GB-Line) Pixel Pre Gain **Address [8Ch], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	G2PGA							
Default	1	0	0	0	0	0	0	0

Bit[7:0] G2PGA : Green(BG-Line) Pixel Pre Gain(/128)

BxPGA [R/W]

Blue Pixel Pre Gain **Address [8Dh], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BxPGA							
Default	1	0	0	0	0	0	0	0

Bit[7:0] BxPGA : Blue Pixel Pre Gain(/128)

ROFST [R/W]

Red Pixel Offset **Address [8Eh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SIGN	ROFST						
Default	0	0	0	0	0	0	0	0

Bit[7] Sign : Sign bit

1 : Minus

0 : Plus

Bit[6:0] ROFST : Red pixel offset absolute value

G1OFST [R/W]

Green1(GR) Pixel Offset **Address [8Fh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SIGN	G1OFST						
Default	0	0	0	0	0	0	0	0

Bit[7] Sign : Sign bit

1 : Minus

0 : Plus

Bit[6:0] G10FST : Green pixel(RG-Line) offset absolute value

G2OFST [R/W]

Green2(GB) Pixel Offset **Address [90h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SIGN	G2OFST						
Default	0	0	0	0	0	0	0	0

Bit[7] Sign : Sign bit

1 : Minus

0 : Plus

Bit[6:0] G2OFST : Green pixel(GB-Line) offset absolute value

BOFST [R/W]

Blue Pixel Offset **Address [91h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SIGN	BOFST						

Default	0	0	0	0	0	0	0	0

Bit[7] Sign : Sign bit

1 : Minus

0 : Plus

Bit[6:0] BOFST : Blue pixel offset absolute value

FILCNTL [R/W]

Filter Control **Address [92h], Default [FEh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	UPFILSEL			DNFILSEL			reserved	
Default	1	1	1	1	1	1	1	0

Bit[7:5] UPFILSEL : 000 – Self Pixel (DPCed)

001 – 8 Median Filter

010 – 4 Median Filter

100 – Diagonal Mean Filter

111 – Min 2 pixel Mean Filter

Bitp[4:2] DNFILSEL : 000 – Self Pixel (DPCed)

001 – 8 Median Filter

010 – 4 Median Filter

100 – Diagonal Mean Filter

111 – Min 2 pixel Mean Filter

GLPFTH [R/W]

Gr,Gb LPF Threshold value **Address [93h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GLPFTH							
Default	0	0	0	0	0	0	0	0

Bit[7:0] GLPFTH :Gr,Gb LPF Threshold value (DPC Block)

GLPFSLOP [R/W]

Gr,Gb LPF Slop Gain **Address [94h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GLPFSLOP							
Default	0	0	0	0	0	0	0	0

Bit[7:0] GLPFSLOP : Gr,Gb LPF Slop Gain (DPC Block)

GLPFEND [R/W]

Gr,Gb LPF End Value **Address [95h], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GLPFEND							
Default	1	1	1	1	1	1	1	1

Bit[7:0] GLPFEND : Gr,Gb LPF End Value (DPC Block)

CLPFTH [R/W]

R,B LPF Threshold Value **Address [96h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CLPFTH							
Default	0	0	0	0	0	0	0	0

Bit[7:0] CLPFTH : R,B LPF Threshold Value (DPC Block)

CLPFSLOP [R/W]

R,B LPF Slop Gain **Address [97h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CLPFSLOP							
Default	0	0	0	0	0	0	0	0

Bit[7:0] CLPFSLOP : R,B LPF Slop Gain (DPC Block)

CLPFEND [R/W]

R,B LPF End Value **Address [98h], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CLPFEND							
Default	1	1	1	1	1	1	1	1

Bit[7:0] CLPFEND : R,B LPF End Value (DPC Block)

LPFSTRT [R/W]

LPF Start Gain **Address [99h], Default [20h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	LPFSTRT							
Default	0	0	1	0	0	0	0	0

Bit[7:0] LPFSTRT : LPF Start Gain(DPC Block)

GLEVEL [R/W]

LPF Up & Down Select **Address [9Ah], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GLEVEL							
Default	0	0	0	0	0	0	0	0

Bit[7:0] GLEVEL : LPF Up & Down Select Level (DPC Block)

BLCFUN [R/W]

BLC Function Register **Address [9Bh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BLCOFST	SELAEB	Reserved					
Default	0	0	0	0	0	0	0	0

Bit[7] BLCOFST : Pixel Offset Cancellation for Fixed BLC

Bit[6] SELAEB : Dark Offset Calibration Block Selection (1: After AWB, 2 : Before AWB)

RxBLCL [R/W]

Red Pixel Dark Value **Address [9Ch], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RxBLCL							
Default	0	0	0	1	0	0	0	0

Bit[7:0] RxBLCL : Red Pixel Dark Value

GrBLCL [R/W]

Green(GR-Line) Pixel Dark Value **Address [9Dh], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GrBLCL							
Default	0	0	0	1	0	0	0	0

Bit[7:0] GrBLCL : Green(GR-Line) Pixel Dark Value

GbBLCL [R/W]

Green(GB-Line) Pixel Dark Value **Address [9Eh], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GbBLCL							
Default	0	0	0	1	0	0	0	0

Bit[7:0] GbBLCL : Green(GB-Line) Pixel Dark Value

BxBLCL [R/W]

Green(GR-Line) Pixel Dark Value **Address [9Fh], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BxBLCL							
Default	0	0	0	1	0	0	0	0

Bit[7:0] BxBLCL : Blue Pixel Dark Value

RxFBLC [R/W]

Red Pixel Fixed Dark Value **Address [A0h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RxFBLC							
Default	0	0	0	1	0	0	0	0

Bit[7:0] RxFBLC : Red Pixel Fixed Dark Value

G1FBLC [R/W]

Green(GR-Line) Pixel Fixed Dark Value **Address [A1h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	G1FBLC							
Default	0	0	0	1	0	0	0	0

Bit[7:0] G1FBLC : Green(GR-Line) Pixel Fixed Dark Value

G2FBLC [R/W]

Green(GR-Line) Pixel Fixed Dark Value **Address [A2h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	G2FBLC							
Default	0	0	0	1	0	0	0	0

Bit[7:0] G2FBLC : Green(GB-Line) Pixel Fixed Dark Value

BxFBLC [R/W]

Blue Pixel Fixed Dark Value **Address [A3h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0

Function	BxFBLC							
Default	0	0	0	1	0	0	0	0

Bit[7:0] BxFBLC : Blue Pixel Fixed Dark Value

SPGA [R/W]

Shading Position Area A **Address [A4h], Default [FDh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SPGJ				SPGI			
Default	1	1	1	1	1	1	0	1

Bit[7:4] SPGJ : Area J shading gain

Bit[3:0] SPGI : Area I shading gain

SPGB [R/W]

Shading Position Area B **Address [A5h], Default [CBh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SPGH				SPGG			
Default	1	1	0	0	1	0	1	1

Bit[7:4] SPGH : Area H shading gain

Bit[3:0] SPGG : Area G shading gain

SPGC [R/W]

Shading Position Area C **Address [A6h], Default [A8h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SPGF				SPGE			
Default	1	0	1	0	1	0	0	0

Bit[7:4] SPGF : Area F shading gain

Bit[3:0] SPGE : Area E shading gain

SPGD [R/W]

Shading Position Area D **Address [A7h], Default [64h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SPGD				SPGC			
Default	0	1	1	0	0	1	0	0

Bit[7:4] SPGD : Area D shading gain

Bit[3:0] SPGC : Area C shading gain

SPGE [R/W]

Shading Position Area E **Address [A8h], Default [21h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SPGB				SPGA			
Default	0	0	1	0	0	0	0	1

Bit[7:4] SPGB : Area B shading gain

Bit[3:0] SPGA : Area A shading gain

RSGX [R/W]

Red Pixel X-axis Shading Gain **Address [A9h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RSGXL				RSGXR			
Default	0	0	0	0	0	0	0	0

Bit[7:4] RSGXL : X-axis R shading gain for left side from horizontal center

Bit[3:0] RSGXR : X-axis R shading gain for right side from horizontal center

RSGY [R/W]

Red Pixel Y-axis Shading Gain **Address [AAh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RSGYT				RSGYB			
Default	0	0	0	0	0	0	0	0

Bit[7:4] RSGYT : Y-axis R shading gain for top side from vertical center

Bit[3:0] RSGYB : Y-axis R shading gain for bottom side from vertical center

GSGX [R/W]

Green Pixel X-axis Shading Gain **Address [ABh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GSGXL				GSGXR			
Default	0	0	0	0	0	0	0	0

Bit[7:4] GSGXL : X-axis G shading gain for left side from horizontal center

Bit[3:0] GSGXR : X-axis G shading gain for right side from horizontal center

GSGY [R/W]

Green Pixel Y-axis Shading Gain **Address [ACh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GSGYT				GSGYB			
Default	0	0	0	0	0	0	0	0

Bit[7:4] GSGYT : Y-axis G shading gain for top side from vertical center

Bit[3:0] GSGYB : Y-axis G shading gain for bottom side from vertical center

BSGX [R/W]

Blue Pixel X-axis Shading Gain **Address [ADh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BSGXL				BSGXR			

Default	0	0	0	0	0	0	0	0

Bit[7:4] BSGXL : X-axis B shading gain for left side from horizontal center

Bit[3:0] BSGXR : X-axis B shading gain for right side from horizontal center

BSGY [R/W]

Blue Pixel Y-axis Shading Gain **Address [AEh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	BSGYT				BSGYB			
Default	0	0	0	0	0	0	0	0

Bit[7:4] BSGYT : Y-axis B shading gain for top side from vertical center

Bit[3:0] BSGYB : Y-axis B shading gain for bottom side from vertical center

SCPX [R/W]

Additional X-axis Shading Gain **Address [AFh], Default [A1h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SCPX							
Default	1	0	1	0	0	0	0	1

Bit[7:0] SCPX : Shading X-axis center position

SCPY [R/W]

Additional Y-axis Shading Gain **Address [B0h], Default [81h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SCPY							
Default	0	0	0	0	0	0	0	0

Bit[7:0] SCPY : Shading Y-axis center position

GMA0 [R/W]

Gamma Point 0 **Address [B1h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA0							
Default	0	0	0	0	0	0	0	0

GMA0 : Gamma point at 0

GMA1 [R/W]

Gamma Point 1 **Address [B2h], Default [08h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA1							
Default	0	0	0	0	1	0	0	0

GMA1 : Gamma point at 16

GMA2 [R/W]

Gamma Point 2 **Address [B3h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA2							
Default	0	0	0	1	0	0	0	0

GMA2 : Gamma point at 32

GMA3 [R/W]

Gamma Point 3 **Address [B4h], Default [1Bh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA3							
Default	0	0	0	1	1	0	1	1

GMA3 : Gamma point at 64

GMA4 [R/W]

Gamma Point 4 **Address [B5h], Default [37h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA4							
Default	0	0	1	1	0	1	1	1

GMA4 : Gamma point at 128

GMA5 [R/W]

Gamma Point 5 **Address [B6h], Default [4Dh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA5							
Default	0	1	0	0	1	1	0	1

GMA5 : Gamma point at 192

GMA6 [R/W]

Gamma Point 6 **Address [B7h], Default [60h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA6							
Default	0	1	1	0	0	0	0	0

GMA6 : Gamma point at 256

GMA7 [R/W]

Gamma Point 7 **Address [B8h], Default [72h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0

Function	GMA7							
Default	0	1	1	1	0	0	1	0

GMA7 : Gamma point at 320

GMA8 [R/W]

Gamma Point 8 **Address [B9h], Default [82h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA8							
Default	1	0	0	0	0	0	1	0

GMA8 : Gamma point at 384

GMA9 [R/W]

Gamma Point 9 **Address [BAh], Default [91h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMA9							
Default	1	0	0	1	0	0	0	1

GMA9 : Gamma point at 448

GMAA [R/W]

Gamma Point A **Address [BBh], Default [A0h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMAA							
Default	1	0	1	0	0	0	0	0

GMAA : Gamma point at 512

GMAB [R/W]

Gamma Point B **Address [BCh], Default [BAh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMAB							
Default	1	0	1	1	1	0	1	0

GMAB : Gamma point at 640

GMAC [R/W]

Gamma Point C **Address [BDh], Default [D3h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMAC							
Default	1	1	0	1	0	0	1	1

GMAC : Gamma point at 768

GMAD [R/W]

Gamma Point D **Address [BEh], Default [EAh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMAD							
Default	1	1	1	0	1	0	1	0

GMAD : Gamma point at 896

GMAE [R/W]

Gamma Point E **Address [BFh], Default [F5h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMAE							
Default	1	1	1	1	0	1	0	1

GMAE : Gamma point at 960

GMAF [R/W]

Gamma Point F **Address [C0h], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GMAF							
Default	1	1	1	1	1	1	1	1

GMAF : Gamma point at 1023

CMA11 [R/W]

Color Matrix Coefficient 11 **Address [C1h], Default [3Bh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA11							
Default	0	0	1	1	1	0	1	1

CMA11 : Color matrix coefficient 11 (x1/64)

2's complement expression

CMA12 [R/W]

Color Matrix Coefficient 12 **Address [C2h], Default [CEh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA12							
Default	1	1	0	0	1	1	1	0

CMA12 : Color matrix coefficient 12 (x1/64)

2's complement expression

CMA13 [R/W]

Color Matrix Coefficient 13 **Address [C3h], Default [F7h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA13							
Default	1	1	1	1	0	1	1	1

CMA13 : Color matrix coefficient 13 (x1/64)

2's complement expression

CMA21 [R/W]

Color Matrix Coefficient 21 **Address [C4h], Default [13h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA21							
Default	0	0	0	1	0	0	1	1

CMA21 : Color matrix coefficient 21 (x1/64)

2's complement expression

CMA22 [R/W]

Color Matrix Coefficient 22 **Address [C5h], Default [25h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA22							
Default	0	0	1	0	0	1	0	1

CMA22 : Color matrix coefficient 22 (x1/64)

2's complement expression

CMA23 [R/W]

Color Matrix Coefficient 23 **Address [C6h], Default [07h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0

Function	CMA23							
Default	0	0	0	0	0	1	1	1

CMA23 : Color matrix coefficient 23 (x1/64)

2's complement expression

CMA31 [R/W]

Color Matrix Coefficient 31 **Address [C7h], Default [F2h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA31							
Default	1	1	1	1	0	0	1	0

CMA31 : Color matrix coefficient 31 (x1/64)

2's complement expression

CMA32 [R/W]

Color Matrix Coefficient 32 **Address [C8h], Default [C7h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA32							
Default	1	1	1	1	0	0	1	0

CMA32 : Color matrix coefficient 32 (x1/64)

2's complement expression

CMA33 [R/W]

Color Matrix Coefficient 33 **Address [C9h], Default [47h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CMA33							
Default	0	0	1	0	0	1	1	1

CMA33 : Color matrix coefficient 33 (x1/64)

2's complement expression

EDGCNT [R/W]

Sharpness Control **Address [CAh], Default [80h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	NCLIP	TYPE		CLPFEN	reserved			
Default	1	0	0	0	0	0	0	0

Bit[7] NCLIP : No Min Max Clip

Bit[6:5] TYPE : 00 – Self Pixel, 01 – 4 Pixel Mean, 10 – 8 Pixel Mean

Bit[4] CLPFEN : Cb Cr LPF Enable Bit

EUGAIN [R/W]

Edge Upper Gain **Address [CBh], Default [20h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EUGAIN							
Default	0	0	1	0	0	0	0	0

EUGAIN : Edge Upper Gain

EDGAIN [R/W]

Edge Down Gain **Address [CCh], Default [40h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EDGAIN							
Default	0	1	0	0	0	0	0	0

EDGAIN : Edge Down Gain

EUCORE [R/W]

Edge Upper Core Value **Address [CDh], Default [04h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EUCORE							
Default	0	0	0	0	0	1	0	0

EUCORE : Edge Upper Core Value

EDCORE [R/W]

Edge Down Core Value **Address [CEh], Default [04h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EDCORE							
Default	0	0	0	0	0	1	0	0

EDCORE : Edge Down Core Value

EUCLIP [R/W]

Edge Enhancement Upper Clip Value **Address [CFh], Default [20h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EUCLIP							
Default	0	0	1	0	0	0	0	0

EUCLIP : Edge Upper clip value

EDCLIP [R/W]

Edge Enhancement Down Clip Value **Address [D0h], Default [20h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EDCLIP							
Default	0	0	1	0	0	0	0	0

EDCLIP : Edge Down clip value

ESTART [R/W]

Edge Suppress Start Gain **Address [D1h], Default [20h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	Reserved	ESTART						
Default	0	0	1	0	0	0	0	0

ESTART : Edge suppress start gain

ESLOP [R/W]

Edge Suppress Slope **Address [D2h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	ESLOP				ESTOP			
Default	0	0	0	1	0	0	0	0

Bit[7:4] ESLOP : Edge suppress slope

Bit[3:0] ESTOP : Edge suppress stop level

EDGLEVEL [R/W]

Edge Threshold Level **Address [D3h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EDGLEVEL							
Default	0	0	0	0	0	0	0	0

Bit[7:0] EDGLEVEL: No Edge Adoption Level

YGAIN [R/W]

Contrast Stretch Gain **Address [D4h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED		YGAIN					
Default	0	0	0	1	0	0	0	0

YGAIN : Contrast stretch gain (x1/16)

CRGAIN [R/W]

Cr Color Saturation Gain **Address [D5h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED		CRGAIN					

Default	0	0	0	1	0	0	0	0

CRGAIN : Cr color saturation gain (x1/16)

CBGAIN [R/W]

Cb Color Saturation Gain **Address [D6h], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	RESERVED		CBGAIN					
Default	0	0	0	1	0	0	0	0

CBGAIN : Cb color saturation gain (x1/16)

BRTCNT [R/W]

Brightness Control **Address [D7h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SIGN	BRTVAL						
Default	0	0	0	0	0	0	0	0

Bit[7] SIGN : Sign bit

0 Positive

1 Negative

Bit[6:0] BRTVAL : Brightness control value (Absolute value : 0~127)

IEFCT [R/W]

Image Effect Control **Address [D8h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	SEPIA	MONO	INVMONO	INVCOLOR	EMBOSS	SKETCH	Reserved	
Default	0	0	0	0	0	0	0	0

Bit[7] SEPIA : Sepia Image Effect Enable Bit (Depend on EFCB & EFCR Value)

Bit[6] MONO: MONO Image Effect Enable Bit

Bit[5] INVMONO: INVMONO Image Effect Enable Bit

Bit[4] INVCOLOR: INVCOLOR Image Effect Enable Bit

Bit[3] EMBOSS: EMBOSS Image Effect Enable Bit

Bit[2] SKETCH: SKETCH Image Effect Enable Bit

EFCB [R/W]

Cb Value for Image Effect **Address [D9h], Default [60h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EFCB							
Default	0	1	1	0	0	0	0	0

Bit[7:0] EFCB : Cb Value for Image Effect

EFCR [R/W]

Cr Value for Image Effect **Address [DAh], Default [A0h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	EFCR							
Default	1	0	1	0	0	0	0	0

Bit[7:0] EFCR : Cr Value for Image Effect

YTOP [R/W]

Luminance Top Clip Value **Address [DBh], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	YTOP							
Default	1	1	1	1	1	1	1	1

Bit[7:0] YTOP : Y top clip value

YBOT [R/W]

Luminance Bottom Clip Value **Address [DCh], Default [10h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0

Function	YBOT							
Default	0	0	0	1	0	0	0	0

Bit[7:0] YBOT : Y bottom clip value

CRTOP [R/W]

Cr Top Clip Value **Address [DDh], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CRTOP							
Default	1	1	1	1	1	1	1	1

Bit[7:0] CRTOP : Cr top clip value

CRBOT [R/W]

Cr Bottom Clip Value **Address [DEh], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CRBOT							
Default	0	0	0	0	0	0	0	0

Bit[7:0] CRBOT : Cr bottom clip value

CBTOP [R/W]

Cb Top Clip Value **Address [DFh], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CBTOP							
Default	1	1	1	1	1	1	1	1

Bit[7:0] CBTOP : Cb top clip value

CBBOT [R/W]

Cb Bottom Clip Value **Address [E0h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	CBBOT							
Default	0	0	0	0	0	0	0	0

Bit[7:0] CBBOT : Cb bottom clip value

GSTRT [R/W]

Color Saturation Suppression Start Gain **Address [E1h], Default [30h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GSTRT							
Default	0	0	1	1	0	0	0	0

Bit[7:0] GSTRT : Suppress start gain point

GSLOP [R/W]

Color Saturation Suppression Slope **Address [E2h], Default [88h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	GSLOP				GENDP			
Default	1	0	0	0	1	0	0	0

Bit[7:4] GLOP : Suppress gain slope (x0.5)

Bit[3:0] GENDP : Suppress gain end point (x8)

WDATH [R/W]

Window Data High Byte **Address [F0h], Default [34h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	WHSH		WHWH		WVSH	WVWH	RESERVED	
Default	0	0	1	1	0	1	0	0

Bit[7:6] WHSH : Window horizontal start high bits

Bit[5:4] WHWH : Window horizontal width high bits

Bit[3] WVSH : Window vertical start high bit

Bit[2] WVWH : Window vertical width high bit

WHSL [R/W]

Window Horizontal Start Low Byte **Address [F1h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	WHSL							
Default	0	0	0	0	0	0	0	0

WHSL : Window horizontal start low byte

WHWL [R/W]

Window Horizontal Width Low Byte **Address [F2h], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	WHWL							
Default	1	1	1	1	1	1	1	1

Bit[7:0] WHWH : Window horizontal width low byte

WVSL [R/W]

Window Vertical Start Low Byte **Address [F3h], Default [00h]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	WVSL							
Default	0	0	0	0	0	0	0	0

Bit[7:0] WVSL : Window horizontal start low byte

WVWL [R/W]

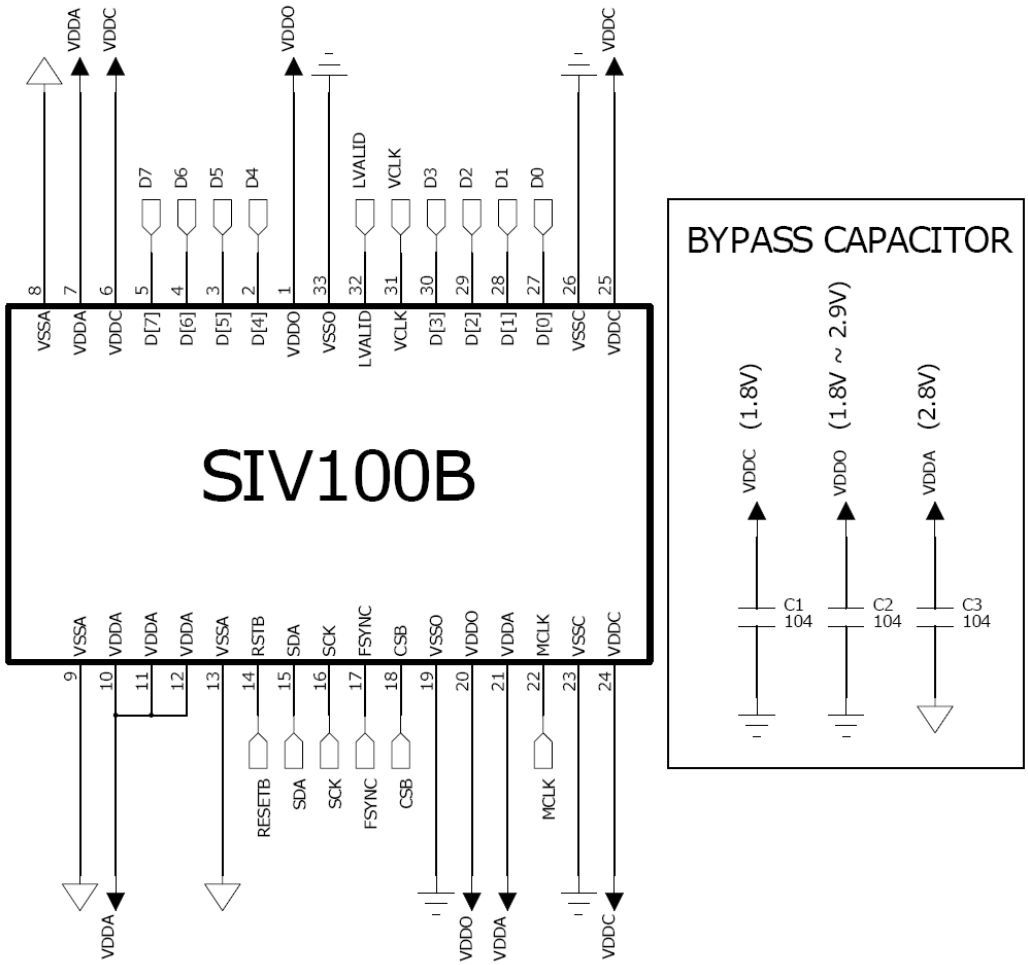
Window Vertical Width Low Byte **Address [F4h], Default [FFh]**

Bits	B7	B6	B5	B4	B3	B2	B1	B0
Function	WVWL							
Default	1	1	1	1	1	1	1	1

Bit[7:0] WVWL : Window vertical width low byte

12. Reference Circuit

Figure 29. SIV100B chip reference circuit



13. Revision History

Table 19. Revision history

Version	Major Revision Items & Remarks	Issued Date
SET-SIV100B-DS070109P	Preliminary release	2007-01-09
SET-SIV100B-DS070228C	Revised for Pin definition, Confidential release	2007-02-28
SET-SIV100B-DS070321C	Errata correction.	2007-03-21
SET-SIV100B-DS070322C	Errata correction.	2007-03-22

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