# MCP Specification

## 1Gb (128Mb x8) NAND Flash
## + 512Mb (16Mb x32) mobile SDR

## Document Title

MCP
1Gb (128Mb x8) NAND Flash / 512Mb (16Mb x32) SDR

## Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.1 | Initial Draft<br>- 1Gb NAND Flash A-Die<br>- 512Mb mobile SDR D-Die | Mar. 2009 | Preliminary |
| 0.2 | Correction<br>- NAND Flash Read ID : 78h -> 74h | Mar. 2009 | Preliminary |

# FEATURES

**[ MCP ]**

- Operation Temperature
  - -30°C ~ 85°C
- Packcage
  - 137-ball FBGA - 10.5x13mm$^2$, 1.2t, 0.8mm pitch
  - Lead Free

**[ NAND Flash ]**

- Multiplane Architecture
- Supply Voltage
  - Vcc = 1.7 - 1.95 V
- Memory Cell Array
  - (512+ 16) Bytes x 32 pages x 8192 blocks
- Page Size
  - (512+ 16 spare) Bytes
- Block Size
  - (16K + 512 spare) Bytes
- Page Read / Program
  - Random access : 15us (max.)
  - Sequential access : 50ns (min.)
  - Page program time : 200us (typ.)
- COPY BACK PROGRAM
  - Automatic block download without latency time
- FAST BLOCK ERASE
  - Block erase time: 1.5ms (typ.)
- ELECTRONIC SIGNATURE
  - 1st cycle : Manufacturer Code
  - 2nd cycle : Device Code
  - 3rd cycle : Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
  - 4th cycle : Page size, Block size, Organization, Spare size
- CHIP ENABLE DON'T CARE
  - Simple interface with microcontroller
- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions.
- DATA RETENTION
  - 100,000 Program/Erase cycles (with 1bit/528byte ECC)
  - 10 years Data Retention

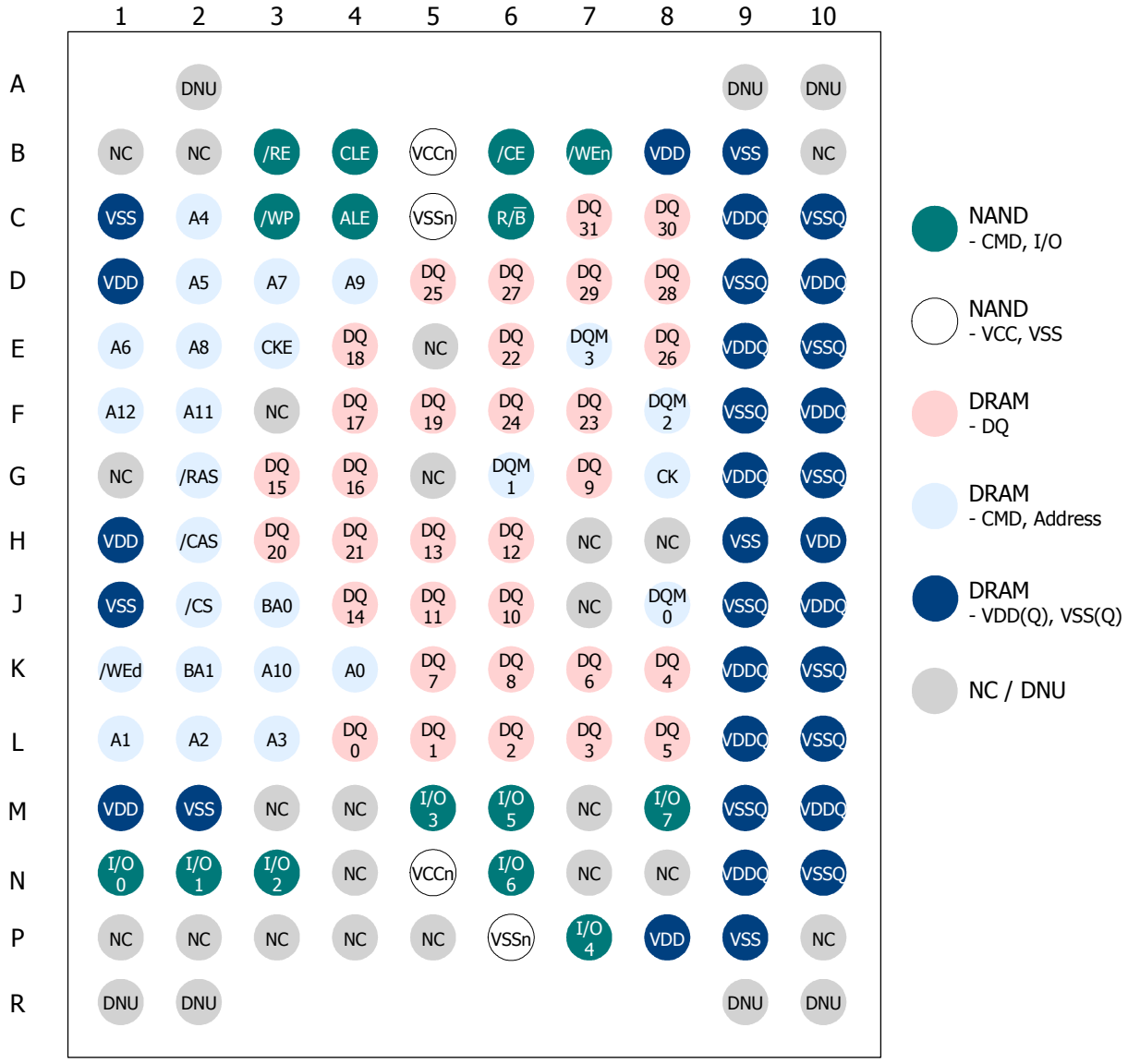
**[ SDR SDRAM ]**

- Standard SDRAM Protocol
- Clock Synchronization Operation
- Multibank Operation : Internal 4 Bank Operation
- VDD / VDDQ = 1.8 V
- Memory Cell Array
  - 4Mb x 4Bank x 32 I/O
- LVCMOS Compatible I/O Interface
- Programmable Burst Length
  - 1, 2, 4, 8 or full page
- Programmable Burst Type
  - sequential or interleaved
- Programmable CAS Latency
- Programmable Drive Strength

## ORDERING INFORMATION

| Part Number | Memory Combination | Operation Voltage | Density | Speed | Package |
|---|---|---|---|---|---|
| H8ACS0EH0ACR-56M | NAND Flash<br>mobile SDR | 1.8V<br>1.8V | 1Gb (128Mb x8)<br>512Mb (16Mb x32) | 50ns<br>166MHz | 137Ball FBGA (Lead Free) |

## Ball Assignment




137 Ball FBGA Package (Top View)

## Pin Description

| SYMBOL | DESCRIPTION |
|---|---|

**< 1Gb (128Mb x8) NAND Flash >**

| | |
|---|---|
| I/O7 ~ I/O0 | Data Input / Output |
| CLE | Command Latch Enable |
| ALE | Address Latch Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{RE}$ | Read Enable |
| $\overline{WP}$ | Write Protect |
| R/$\overline{B}$ | Ready / Busy Out |
| VCC | Supply Voltage |
| VSS | Ground |

**< 512Mb (16Mb x32) mobile SDR >**

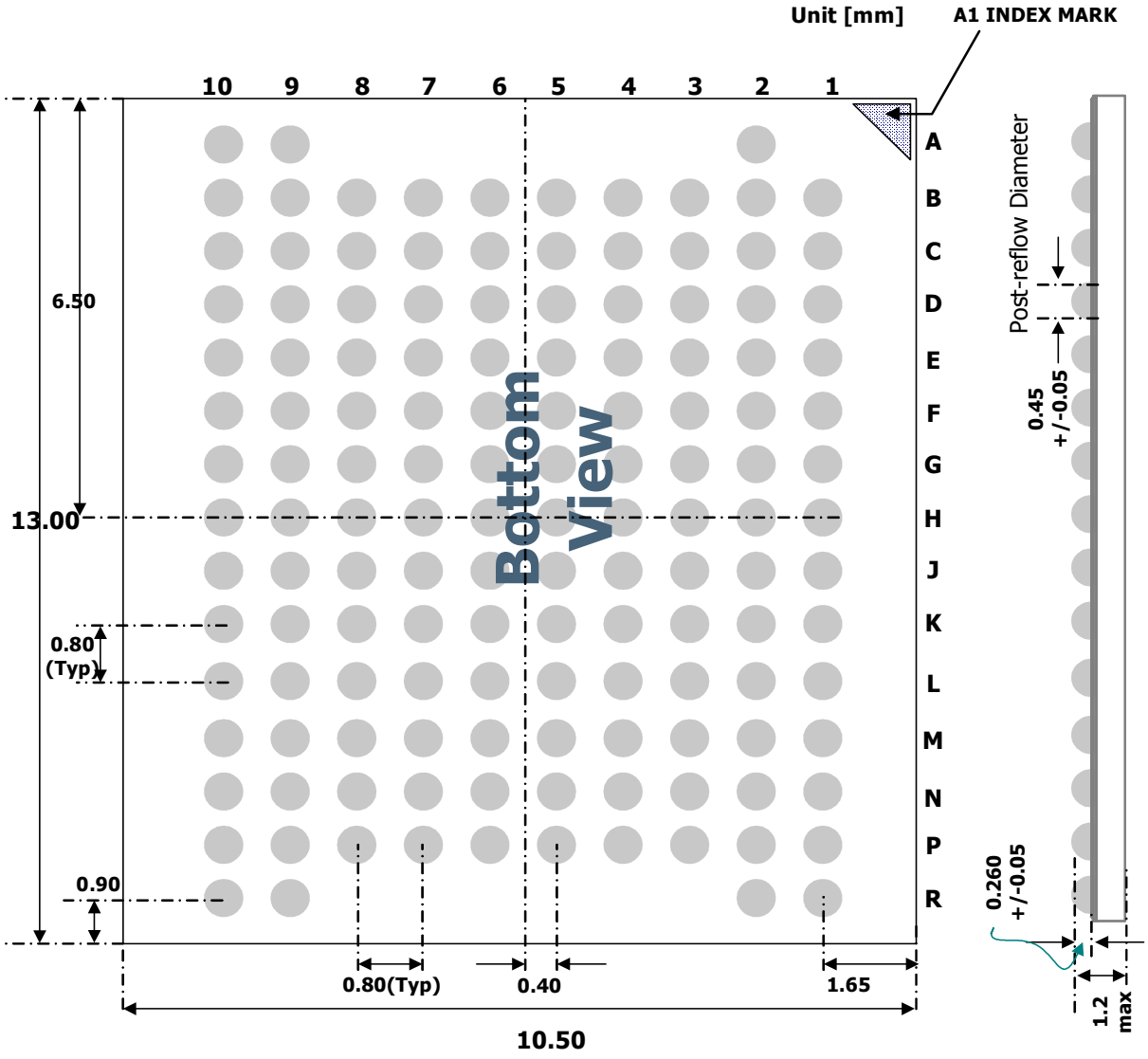
| | |
|---|---|
| CK | Clock Input |
| CKE | Clock Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Command Inputs |
| BA0, BA1 | Bank Address Inputs |
| A0 ~ A12 | Address Inputs |
| DQ0 ~ DQ31 | Data Bus |
| DQM0~DQM3 | Input Data Mask |
| VDD | Power Supply |
| VSS | Ground |
| VDDQ | I/O Power Supply |
| VSSQ | I/O Ground |

**< Common >**

| | |
|---|---|
| DNU | Do Not Use |
| NC | No Connection |

## PACKAGE INFORMATION

### 137 Ball 0.8mm pitch 10.5mm x 13.0mm (t=1.2mm) FBGA



# 1Gb (128Mb x8) NAND FLASH A-Die

# 1. SUMMARY DESCRIPTION

The Hynix NAND Flash is a 1Gbit with spare 32Mbit capacity. The device is offered in 1.8V Vcc Power Supply, and with x8 I/O interface.

Its NAND cell provides the most cost-effective solution for the solid state mass storage market.

The device is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 8192 blocks, composed by 32 pages consisting in two NAND sturctures of 16 series connected Flash cells. A program operation allows to write the 512-byte page in typical 200 us and an erase operation can be performed in typical 1.5 ms on a 16 Kbyte block.

Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ input. The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

The copy back function allows the optimization of defective blocks management. When a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

Even the write-intensive systems can take advantage of the H27S1G8S2A Series extended reliability of 100K program/ erase cycles by supporting ECC (Error Correcting Code) with real time mapping-out algorithm. The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

## 1.1 Product List

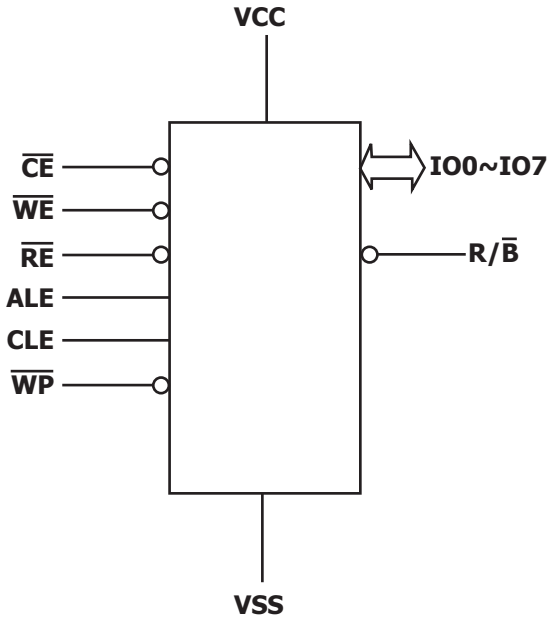



**Figure1: Logic Diagram**

| | |
|---|---|
| IO7 - IO0 | Data Inputs / Outputs |
| CLE | Command latch enable |
| ALE | Address latch enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{RE}$ | Read Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{WP}$ | Write Protect |
| R/$\overline{B}$ | Ready / Busy |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |

**Table 1: Signal Names**

## 1.2 PIN DESCRIPTION

| Pin Name | Description |
|---|---|
| IO0-IO7 | **DATA INPUTS/OUTPUTS**<br>The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled. |
| CLE | **COMMAND LATCH ENABLE**<br>This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$). |
| ALE | **ADDRESS LATCH ENABLE**<br>This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$). |
| $\overline{CE}$ | **CHIP ENABLE**<br>This input controls the selection of the device. When the device is busy $\overline{CE}$ low does not deselect the memory. |
| $\overline{WE}$ | **WRITE ENABLE**<br>This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$. |
| $\overline{RE}$ | **READ ENABLE**<br>The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one. |
| $\overline{WP}$ | **WRITE PROTECT**<br>The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations. |
| R/$\overline{B}$ | **READY BUSY**<br>The Ready/Busy output is an Open Drain pin that signals the state of the memory. |
| VCC | **SUPPLY VOLTAGE**<br>The VCC supplies the power for all the operations (Read, Write, Erase). |
| VSS | GROUND |
| NC | NO CONNECTION |

**Table 2: Pin Description**

**NOTE:**

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
2. An internal voltage detector disables all functions whenever VCC is below 1.8V to protect the device from any involuntary program/erase during power transitions.

| | IO0 | IO1 | IO2 | IO3 | IO4 | IO5 | IO6 | IO7 |
|---|---|---|---|---|---|---|---|---|
| **1st Cycle** | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| **2nd Cycle** | A9 | A10 | A11 | A12 | A13 | A14 | A15 | A16 |
| **3rd Cycle** | A17 | A18 | A19 | A20 | A21 | A22 | A23 | A24 |
| **4th Cycle** | A25 | A26 | L [1] | L [1] | L [1] | L [1] | L [1] | L [1] |

**Table 3: Address Cycle Map(x8)**

**NOTE:**

1. L must be set to Low
2. A8 is set to LOW or High by the Read 1 Command(00h or 01h).

| Density | Plane Address | Block Address | Page Address | Column Address |
|---|---|---|---|---|
| 1 Gbit | A26, A25 | A24 ~ A14 | A13 ~ A9 | A7 ~ A0 |

**Table 4: Address Role**

| FUNCTION | 1st CYCLE | 2nd CYCLE | 3rd CYCLE | 4th CYCLE | Acceptable command during busy |
|---|---|---|---|---|---|
| **READ 1** | 00h / 01h | - | - | - | |
| **READ 2** | 50 h | - | - | - | |
| **READ ID** | 90h | - | - | - | |
| **RESET** | FFh | - | - | - | Yes |
| **PAGE PROGRAM** | 80h | 10h | - | - | |
| **COPY BACK PROGRAM [1]** | 00h | 8Ah | (10h) | - | |
| **BLOCK ERASE** | 60h | D0h | - | - | |
| **READ STATUS REGISTER** | 70h | - | - | - | Yes |

**Table 5: Command Set**

**NOTE**

1. The program confirm command (10h) can either be excuted or ignored during copy back program

| CLE | ALE | $\overline{CE}$ | $\overline{WE}$ | $\overline{RE}$ | $\overline{WP}$ | MODE | |
|---|---|---|---|---|---|---|---|
| H | L | L | Rising | H | X | Read Mode | Command Input |
| L | H | L | Rising | H | X | | Address Input |
| H | L | L | Rising | H | H | Write Mode | Command Input |
| L | H | L | Rising | H | H | | Address Input |
| L | L | L | Rising | H | H | Data Input | |
| L | L | L [1] | H | Falling | X | Sequential Read and Data Output | |
| L | L | L | H | H | X | During Read (Busy) | |
| X | X | X | X | X | H | During Program (Busy) | |
| X | X | X | X | X | H | During Erase (Busy) | |
| X | X | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/Vcc | Stand By | |

**Table 6: Mode Selection**

**NOTE:**

1. With the $\overline{CE}$ high during latency time does not stop the read operation

# 2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

## 2.1 Command Set.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/ erase) the Write Protect pin must be high. See Figure 7 and Table 8 for details of the timings requirements.

## 2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See Figure 8 and Table 8 for details of the timings requirements.

## 2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 9 and Table 8 for details of the timings requirements.

## 2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 10, 11, 13, 14 ,15 and Table 8 for details of the timings requirements.

## 2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modifying operation does not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

## 2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

# 3. DEVICE OPERATION

## 3.1 Page Read.

Upon initial device power up, the device defaults to Read1(00h/01h) mode. This operation is also initiated by writing 00h to the command register along with followed by the four address input cycles. Once the command is latched, it does not need to be written for the following page read operation.

Three types of operations are available: random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes (x8 device) of data within the selected page are transferred to the data registers in less than access random read time tR. The system controller can detect the completion of this data transfer tR by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50 ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.

After the data of last column address is clocked out, the next page is automatically selected for sequential row read.

Waiting tR again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area (Refer to Figure 19) . Writing the Read2 command user may selectively access the spare area of bytes 512 to 527. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored.

Unless the operation is aborted, the page address is automatically incremented for sequential row

Read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figure 9 to 11 show typical sequence and timings for each read operation.

## 3.2 Page Program.

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operations within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to Figure 20.

The data-loading sequence begins by inputting the Serial Data Input command (80h), followed by the four address input cycles (Refer to Table 3 for details) and then serial data loading. The Page Program confirm command (10h) starts the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal Program Erase Controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked as specified in Figure 12.

The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

### 3.3 Block Erase.

The Erase operation is done on a block (16K Byte) basis. It consists of an Erase Setup command (60h), a Block address loading and an Erase Confirm Command (D0h). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

The block address loading is accomplished three cycles. Only block addresses(from A14 upwards , the highest address depending on the device density; Refer to Table 4 for further info) are needed while A9 to A13 is ignored.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal Program Erase Controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure 13 details the sequence.

### 3.4 Copy-Back Program.

The copy-back program is provided to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without using an external memory. Since the time-consuming sequential-reading and its reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is not needed to actually begin the programming operation. For backward-compatibility, issuing Program Confirm command during copy-back does not prevent correct device operation.

Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Plane address must be the same between source and target page(Refer to Table 4 for details).

When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation.
Figure 14 shows the command sequence for the copy-back operation.

### 3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the read, program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last (see figure Figure 8). This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 13 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

### 3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (20h), the device code, A5h and 00h The command register remains in Read ID mode until further commands are issued to it. Figure 15 shows the operation sequence, while Tables 14 to 15 explain the byte meaning.

### 3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 16 below.

# 4. OTHER FEATURES

## 4.1 Data Protection

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below $V_{LKO}$ (1.1 V for 1.8 V version) . $\overline{WP}$ pin provides hardware protection and is recommended to be kept at $V_{IL}$ during power-up and power-down. A recovery time of minimum 10 us is required before internal circuit gets ready for any command sequences as shown in Figure 17. The two-step command sequence for program/erase provides additional software protection.

## 4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy ($I_{busy}$), an appropriate value can be obtained with the following reference chart in Figure 18. Its value can be determined by the following guidance.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Valid Block Number | $N_{VB}$ | 8032 | 8192 | Blocks |

**Table 7: Valid Blocks Number**

**NOTE:**

1. The 1st block is guaranteed to be a valid block up to 1K cycles with ECC. (1bit/528bytes)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| | | 1.8V | |
| $T_A$ | Ambient Operating Temperature (Mobile Temperature Range) | -30 to 85 | ℃ |
| $T_{BIAS}$ | Temperature Under Bias | -50 to 125 | ℃ |
| $T_{STG}$ | Storage Temperature | -65 to 150 | ℃ |
| $V_{IO}$(2) | Input or Output Voltage | -0.6 to 2.7 | V |
| Vcc | Supply Voltage | -0.6 to 2.7 | V |

**Table 8: Absolute maximum ratings**

**NOTE:**

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

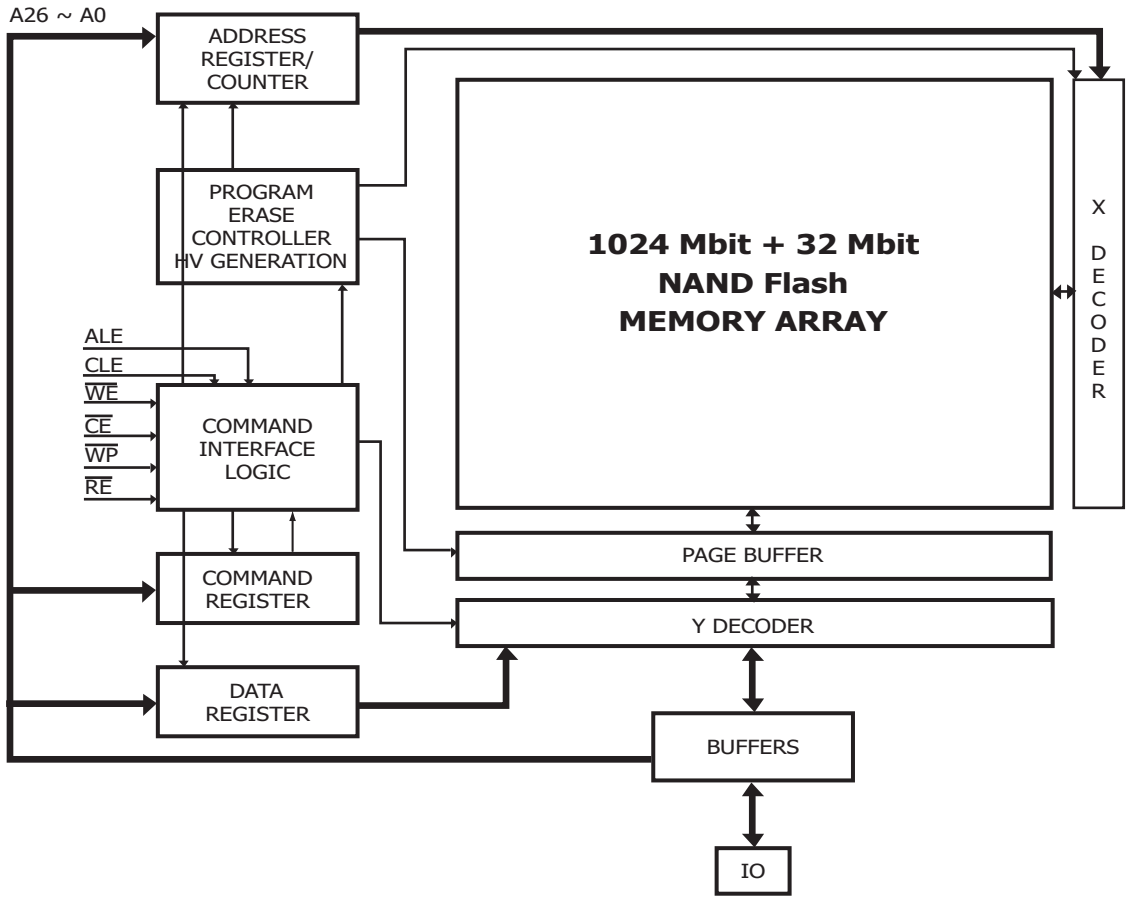



**Figure 3 : Block Diagram**

| Parameter | | Symbol | Test Conditions | 1.8Volt | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Operating Current | Sequential Read | $I_{CC1}$ | $t_{RC}$=50ns, $\overline{CE}$=$V_{IL}$, $I_{OUT}$=0mA | - | 10 | 20 | mA |
| | Program | $I_{CC2}$ | - | - | 10 | 20 | mA |
| | Erase | $I_{CC3}$ | - | - | 10 | 20 | mA |
| Stand-by Current (TTL) | | $I_{CC4}$ | $\overline{CE}$=$V_{IH}$, $\overline{WP}$=0V/Vcc | - | - | 1 | mA |
| Stand-by Current (CMOS) | | $I_{CC5}$ | $\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc | - | 10 | 50 | uA |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 to Vcc (max) | - | - | ± 10 | uA |
| Output Leakage Current | | $I_{LO}$ | $V_{OUT}$ =0 -to Vcc (max) | - | - | ± 10 | uA |
| Input High Voltage | | $V_{IH}$ | - | Vccx0.8 | - | Vcc+0.3 | V |
| Input Low Voltage | | $V_{IL}$ | - | -0.3 | - | Vccx0.2 | V |
| Output High Voltage Level | | $V_{OH}$ | $I_{OH}$=-100uA | Vcc-0.1 | - | - | V |
| Output Low Voltage Leve | | $V_{OL}$ | $I_{OL}$=100uA | - | - | 0.1 | V |
| Output Low Current (R/$\overline{B}$) | | $I_{OL}$ (R/$\overline{B}$) | $V_{OL}$=0.2V | 3 | 4 | - | mA |
| Vcc supply voltage (erase and program) lockout | | $V_{LKO}$ | - | - | 1.1 | - | V |

**Table 9: DC and Operating Characteristics**

| Parameter | Value |
|---|---|
| | 1.8Volt |
| Input Pulse Levels | 0V to Vcc |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | Vcc / 2 |
| Output Load (1.7V - 1.95V) | 1 TTL GATE and CL=30pF |

**Table 10: AC Conditions**

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input / Output Capacitance | $C_{I/O}$ | $V_{IL}$=0V | - | 10 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 10 | pF |

**Table 11: Pin Capacitance ($T_A$ =25℃, F=1.0MHz)**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Program Time | | $t_{PROG}$ | - | 200 | 700 | us |
| Number of partial Program Cycles in the same page | Main Array | NOP | - | - | 1 | Cycles |
| | Spare Array | | - | - | 2 | |
| Block Erase Time | | $t_{BERS}$ | - | 1.5 | 3 | ms |

**Table 12: Program / Erase Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CLE Setup time | $t_{CLS}$ | 25 | | ns |
| CLE Hold time | $t_{CLH}$ | 10 | | ns |
| $\overline{CE}$ setup time | $t_{CS}$ | 35 | | ns |
| $\overline{CE}$ hold time | $t_{CH}$ | 10 | | ns |
| $\overline{WE}$ pulse width | $t_{WP}$ | 25 | | ns |
| ALE setup time | $t_{ALS}$ | 25 | | ns |
| ALE hold time | $t_{ALH}$ | 10 | | ns |
| Data setup time | $t_{DS}$ | 20 | | ns |
| Data hold time | $t_{DH}$ | 10 | | ns |
| Write Cycle time | $t_{WC}$ | 45 | | ns |
| $\overline{WE}$ High hold time | $t_{WH}$ | 15 | | ns |
| Data Transfer from Cell to register | $t_{R}$ | | 15 | us |
| ALE to $\overline{RE}$ Delay (ID Read) | $t_{AR1}$ | 10 | | ns |
| CLE to $\overline{RE}$ Delay | $t_{CLR}$ | 10 | | ns |
| Ready to $\overline{RE}$ Low | $t_{RR}$ | 20 | | ns |
| $\overline{RE}$ Pulse Width | $t_{RP}$ | 25 | | ns |
| $\overline{WE}$ High to Busy | $t_{WB}$ | | 100 | ns |
| Read Cycle Time | $t_{RC}$ | 50 | | ns |
| $\overline{RE}$ Access Time | $t_{REA}$ | | 30 | ns |
| $\overline{RE}$ High to Output High Z | $t_{RHZ}$ | | 30 | ns |
| $\overline{CE}$ High to Output High Z | $t_{CHZ}$ | | 20 | ns |
| $\overline{RE}$ or $\overline{CE}$ high to Output hold | $T_{OH}$ | 10 | | |
| $\overline{RE}$ High Hold Time | $T_{REH}$ | 15 | | ns |
| Output High Z to $\overline{RE}$ low | $t_{IR}$ | 0 | | ns |
| $\overline{WE}$ High to $\overline{RE}$ low | $t_{WHR}$ | 60 | | ns |
| Device Resetting Time (Read / Program / Erase) | $t_{RST}$ | | 5/10/500 (1,2) | us |
| Last RE High to BUSY (at sequential read) | $t_{RB}$ | | 100 | ns |
| $\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$) | $t_{CRY}$ | | 60+tr(1) | ns |
| $\overline{CE}$ High hold time (at the last serial read) | $t_{CEH}$ | 100(3) | | ns |

**Table 13: AC Timing Characteristics**

**NOTE**
1. The time to Ready depends on the value of the pull-up resistor tied to R/$\overline{B}$ pin.
2. If Reset Command (FFh) is issued at Ready state, the device goes into Busy for maximum 5 us.
3. To break the sequential read cycle. $\overline{CE}$ must be held high for a time longer than $t_{CEH}$

| IO | Page Program | Block Erase | Read | Cache Read | CODING |
|---|---|---|---|---|---|
| 0 | Pass / Fail | Pass / Fail | NA | NA | Pass: '0' Fail: '1' |
| 1 | NA | NA | NA | NA | Pass: '0' Fail: '1' (Only for Cache Program, else Don't care) |
| 2 | NA | NA | NA | NA | - |
| 3 | NA | NA | NA | NA | - |
| 4 | NA | NA | NA | NA | - |
| 5 | Ready/Busy | Ready/Busy | Ready/Busy | P/E/R Controller Bit | Active: '0' Idle:'1' |
| 6 | Ready/Busy | Ready/Busy | Ready/Busy | Ready/Busy | Busy: '0' Ready:'1' |
| 7 | Write Protect | Write Protect | Write Protect | NA | Protected: '0' Not Protected: '1' |

**Table 14: Status Register Coding**

| DEVIIDENTIFIER CYCLE | DESCRIPTION |
|---|---|
| 1st | Manufacturer Code |
| 2nd | Device Identifier |
| 3rd | Internal chip number, cell Type, Number of Simultaneously Programmed pages. |
| 4th | Page size, spare size, Block size, Organization |

**Table 15: Debice Identifier Coding**

| Device | Voltage | Bus Width | 1st cycle (Manufacture Code) | 2nd cycle (Device Code) | 3rd Code | 4th Code |
|---|---|---|---|---|---|---|
| NAND Flash | 1.8V | x8 | ADh | 74h | A5h | 00h |

**Table 16: Read ID Data Table**

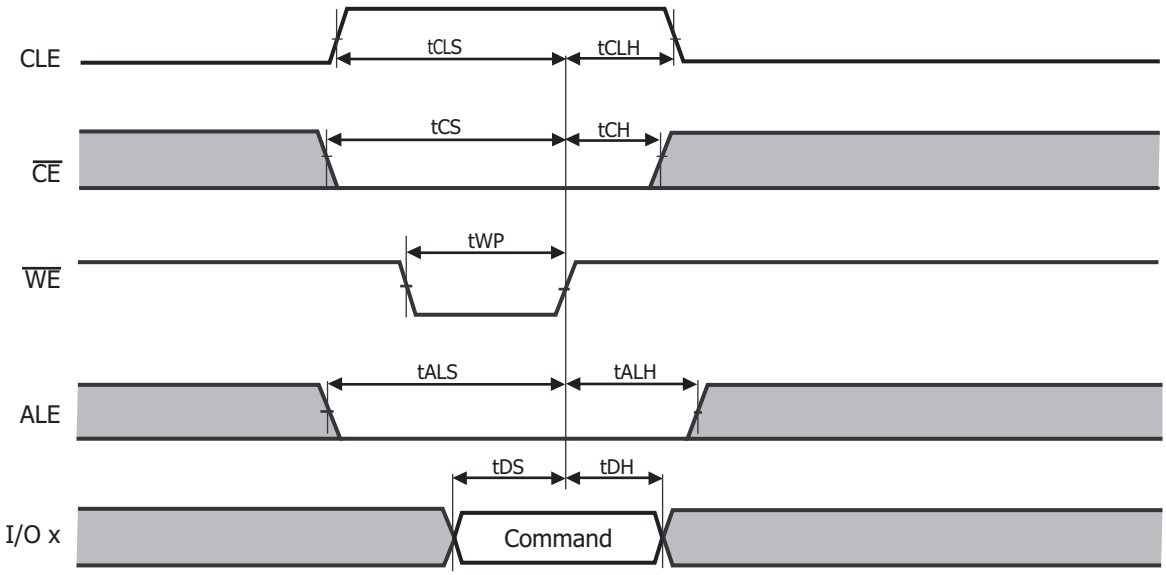



**Figure 4: Command Latch Cycle**

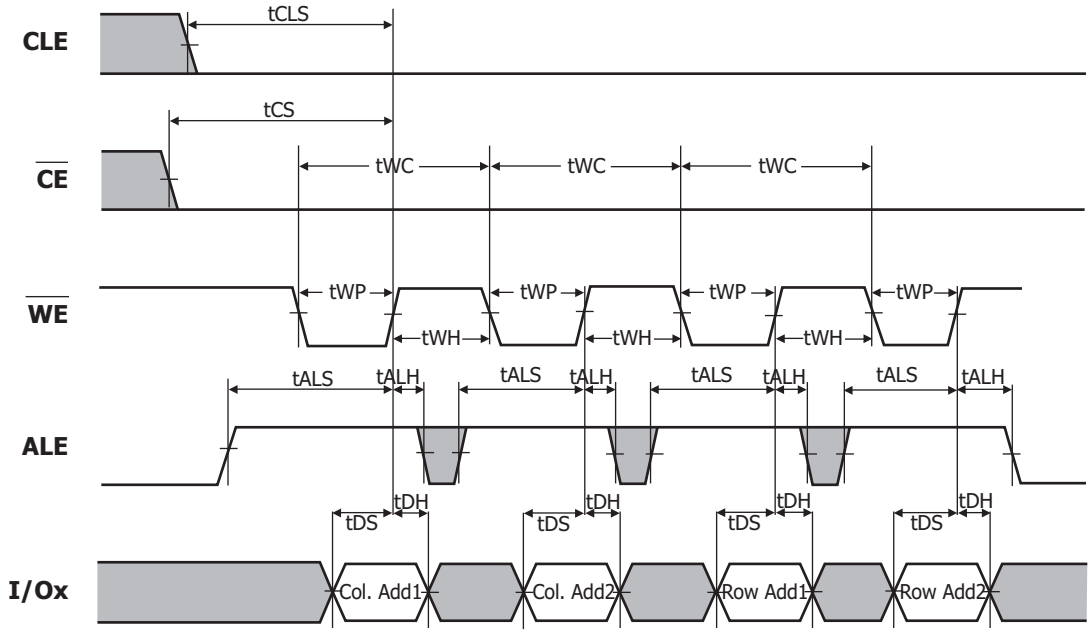
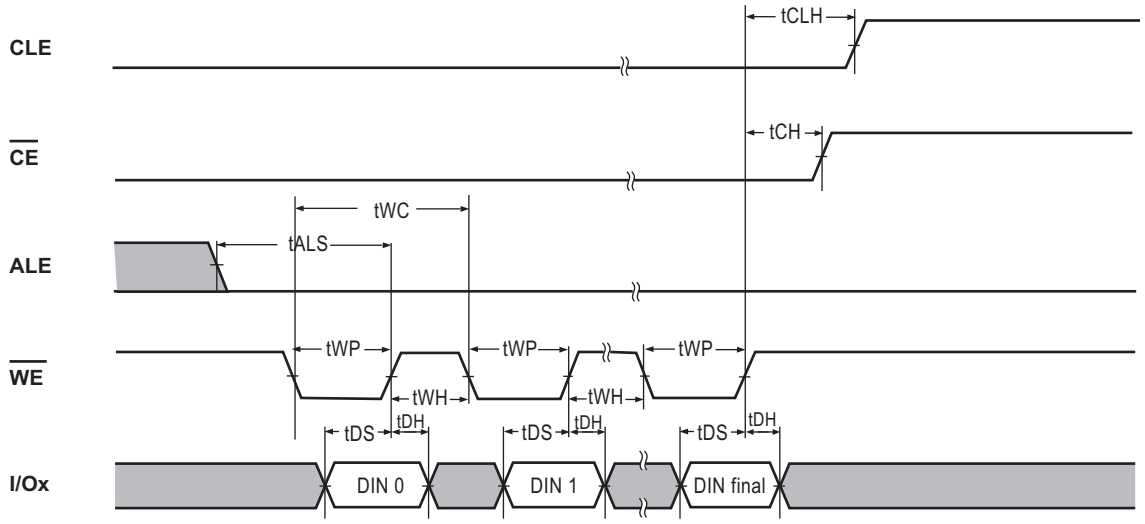
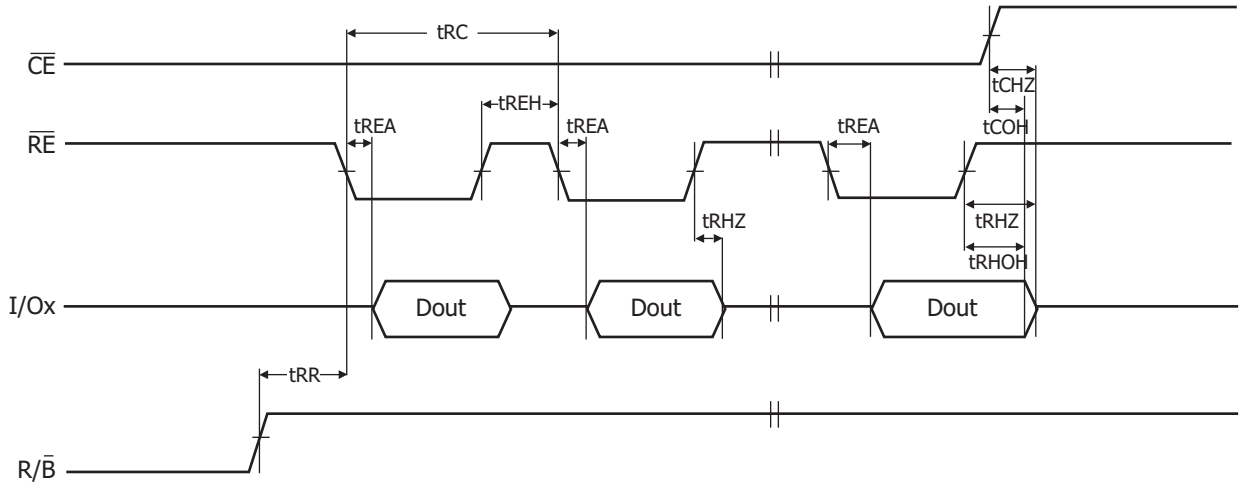



**Figure 5: Address Latch Cycle**




Notes: DIN final means 2,112Bytes (x8)

**Figure 6. Input Data Latch Cycle**




Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33MHz.

**Figure 7: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)**

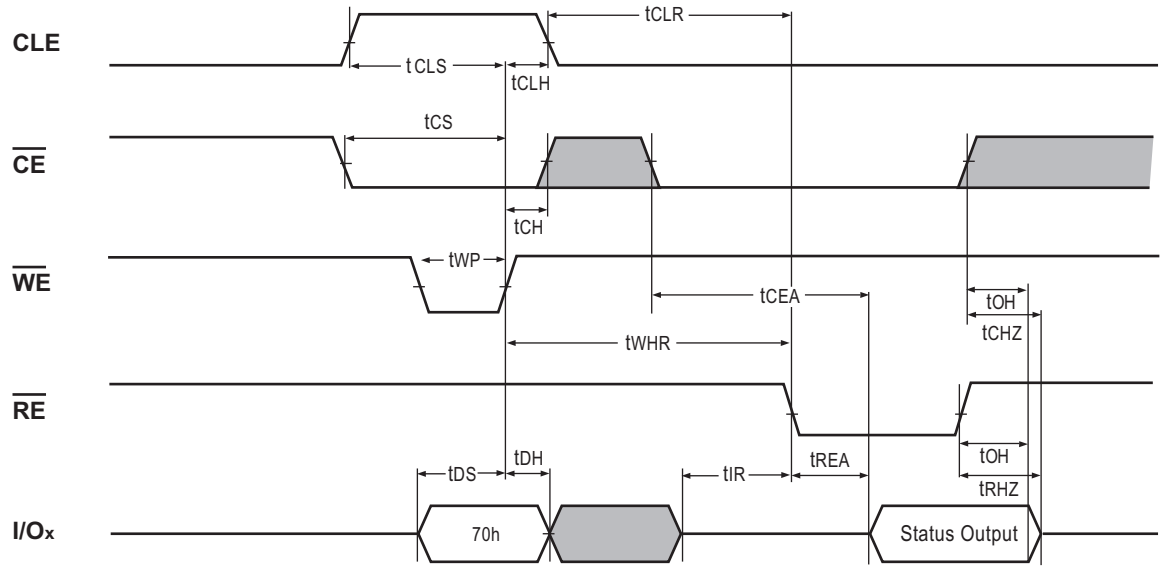



**Figure 8: Status Read Cycle**

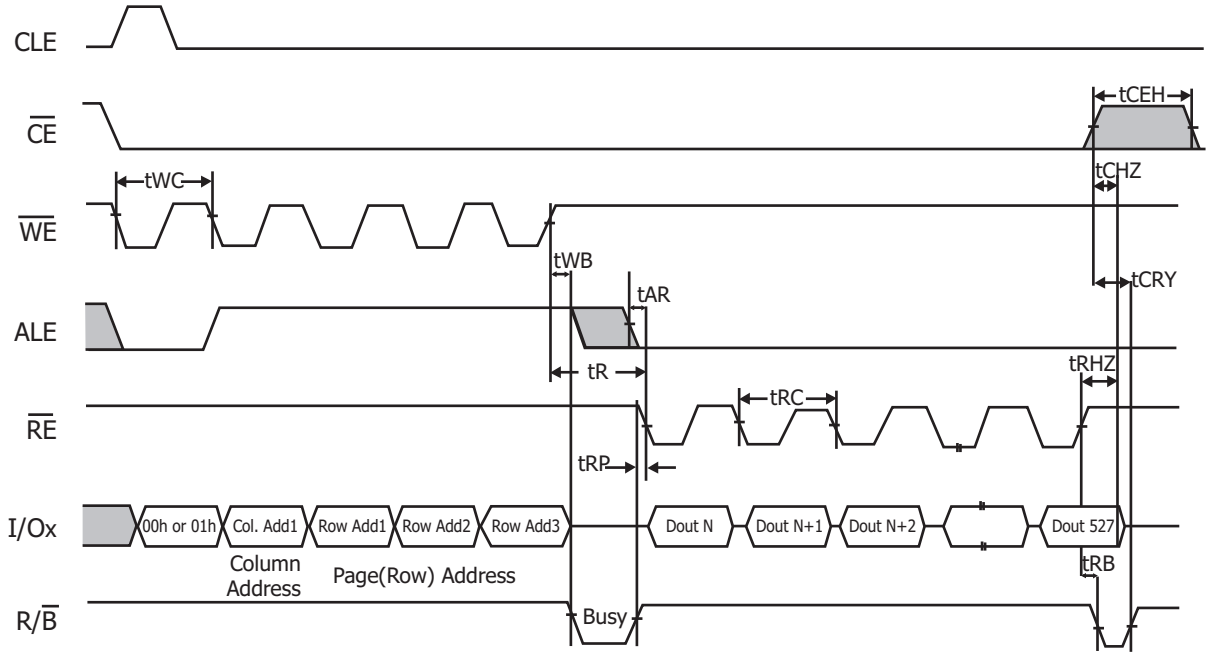



**Figure 9: Read 1 Operation (Read One Page)**

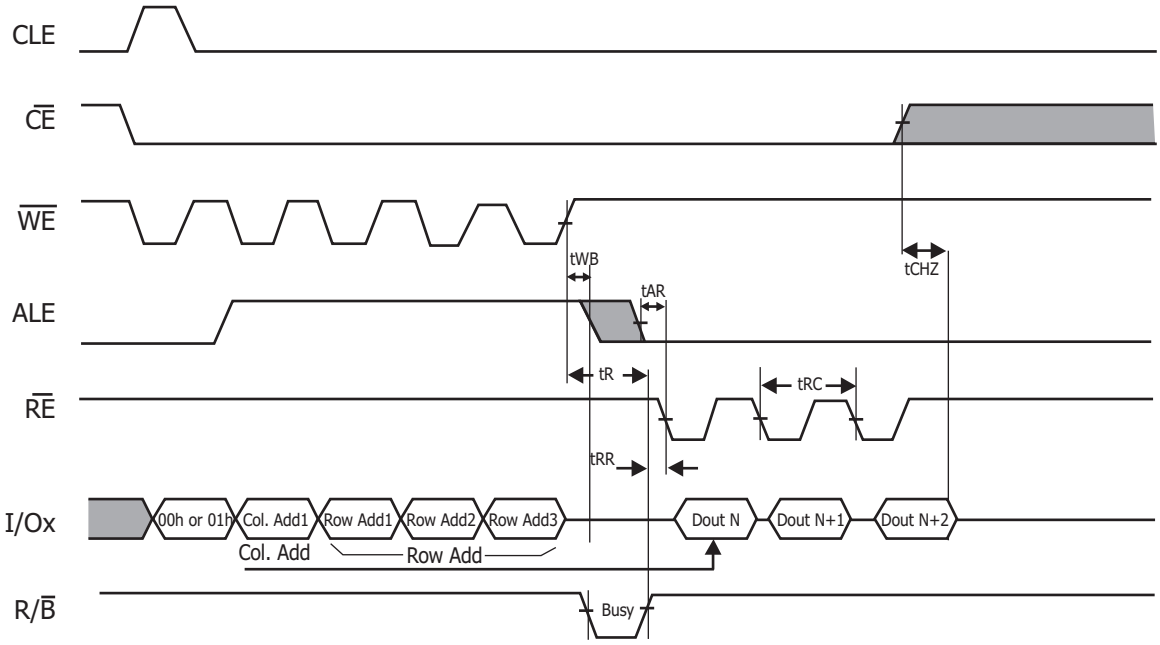



**Figure 10: Read 1 Operation intercepted by $\overline{CE}$**

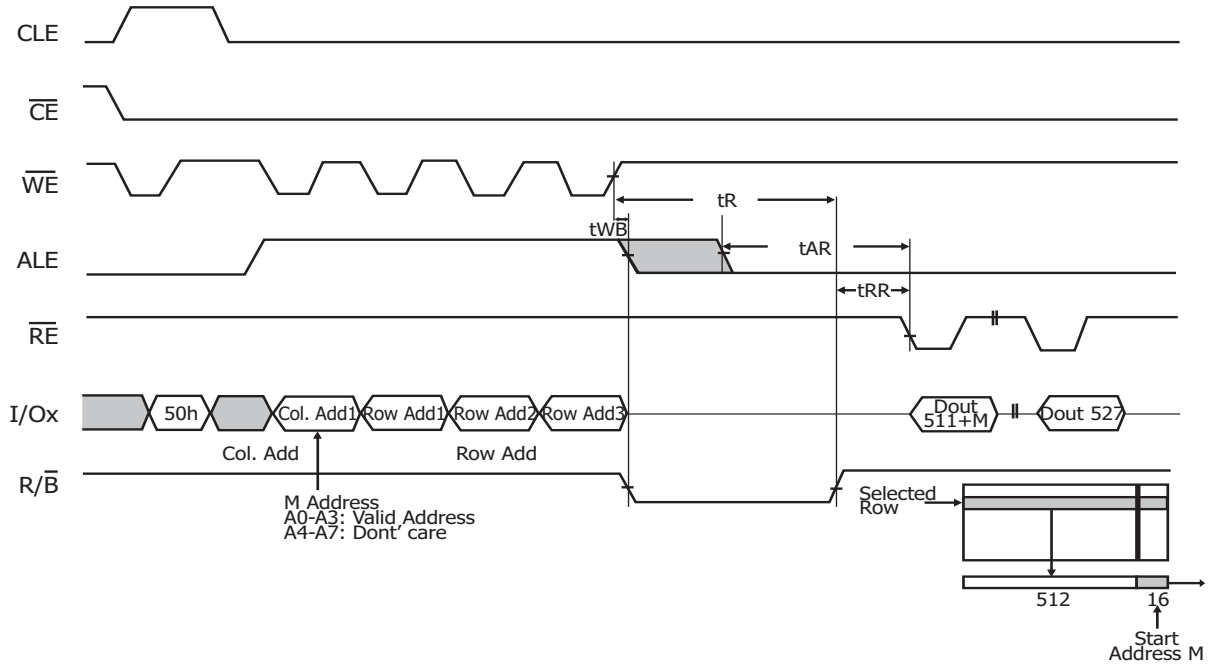



**Figure 11 : Read 2 Operation (Read One Page)**

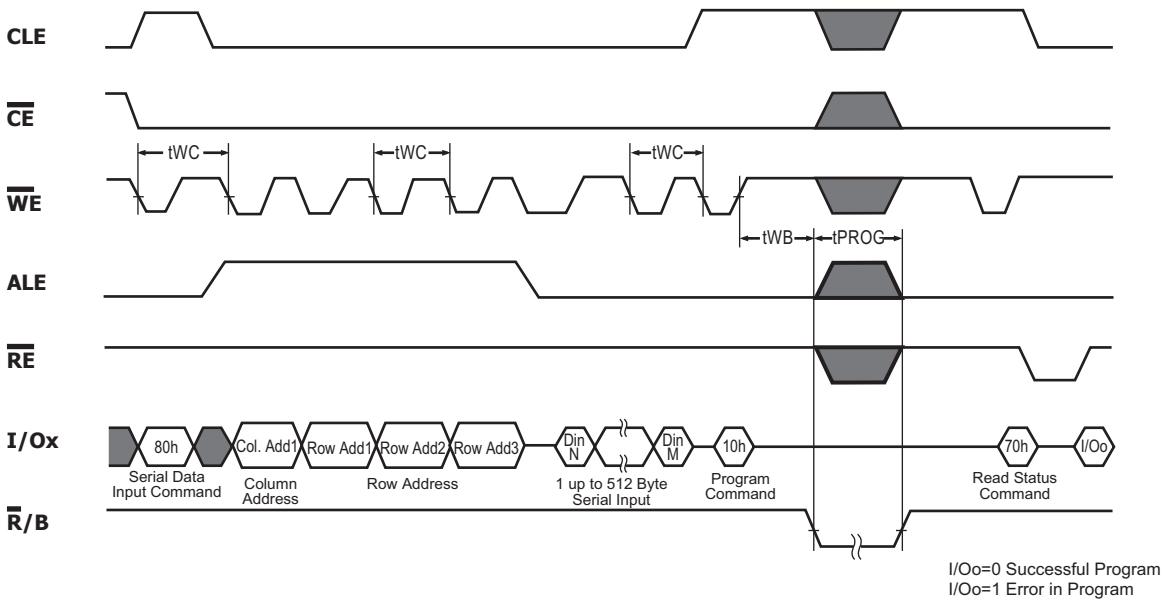



**Figure 12: Page Program Operation**

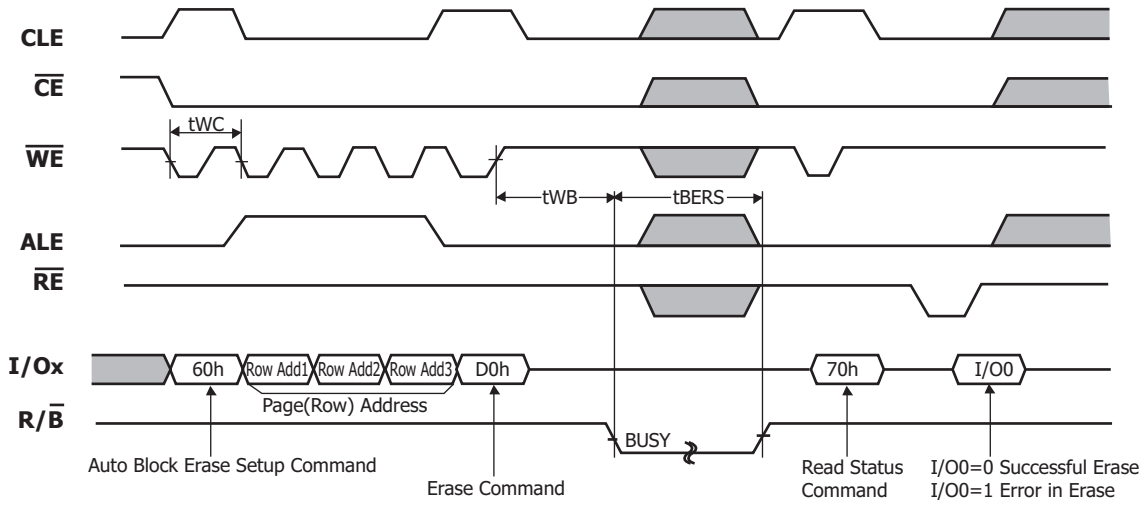
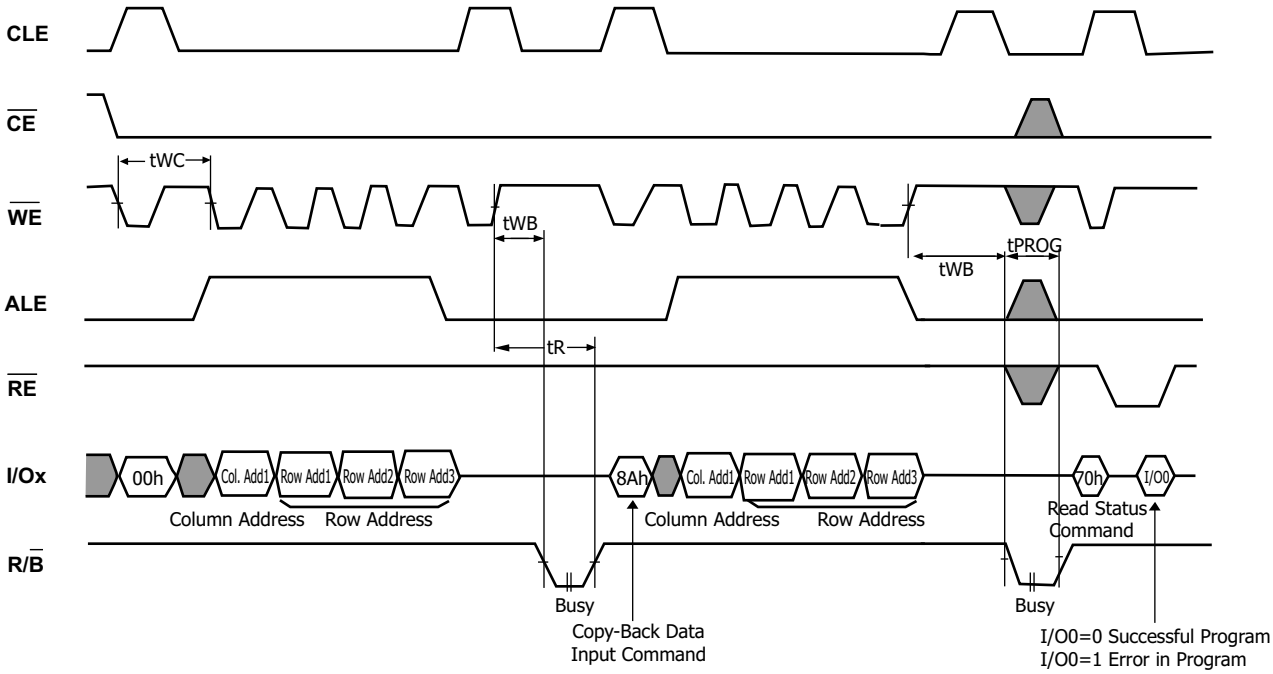



**Figure 13: Block Erase Operation (Erase One Block)**




Note : tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge fo first data cycle.

**Figure 14: Copy Back Program**

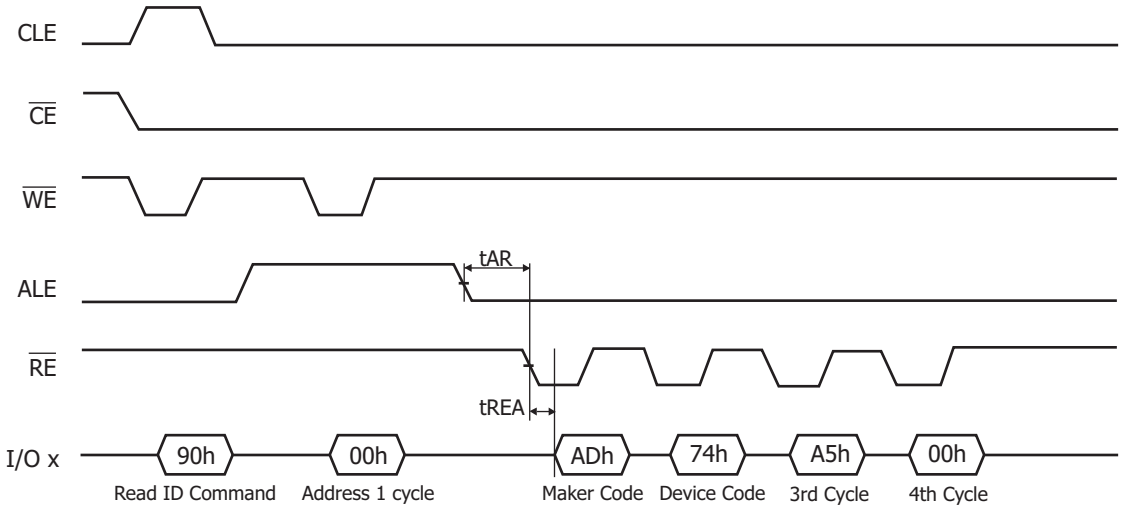



**Figure 15: Read ID Operation**

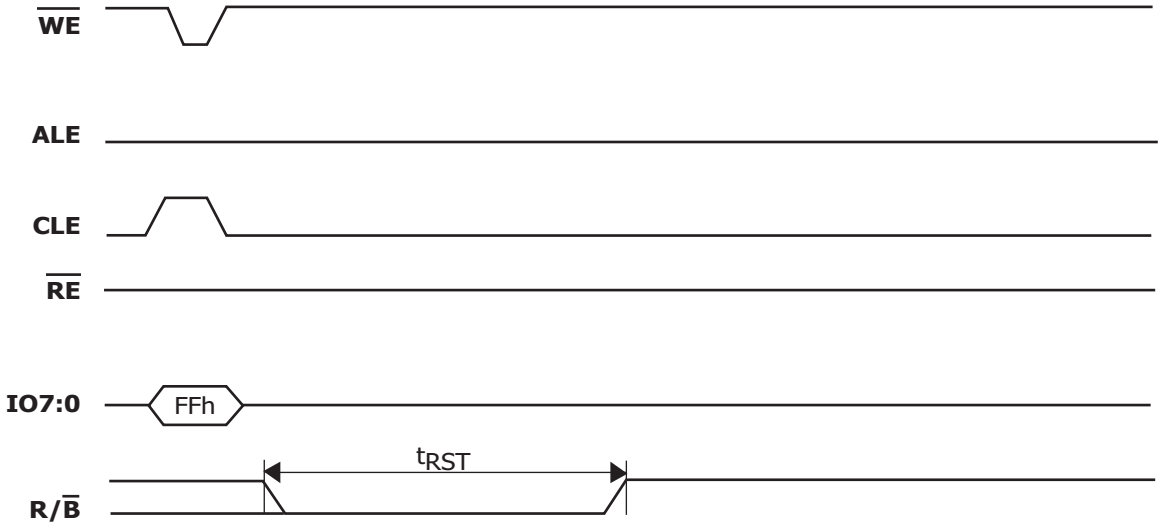



**Figure 16: Reset Operation**

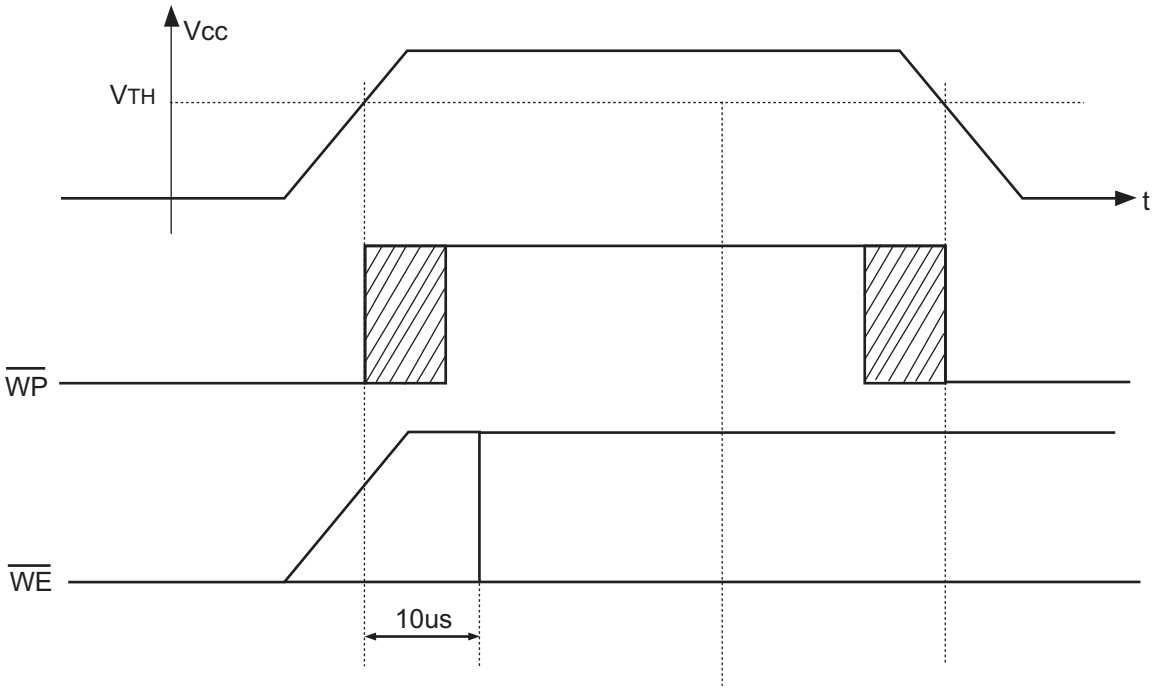



**Figure 17: Power On and Data Protection Timing**

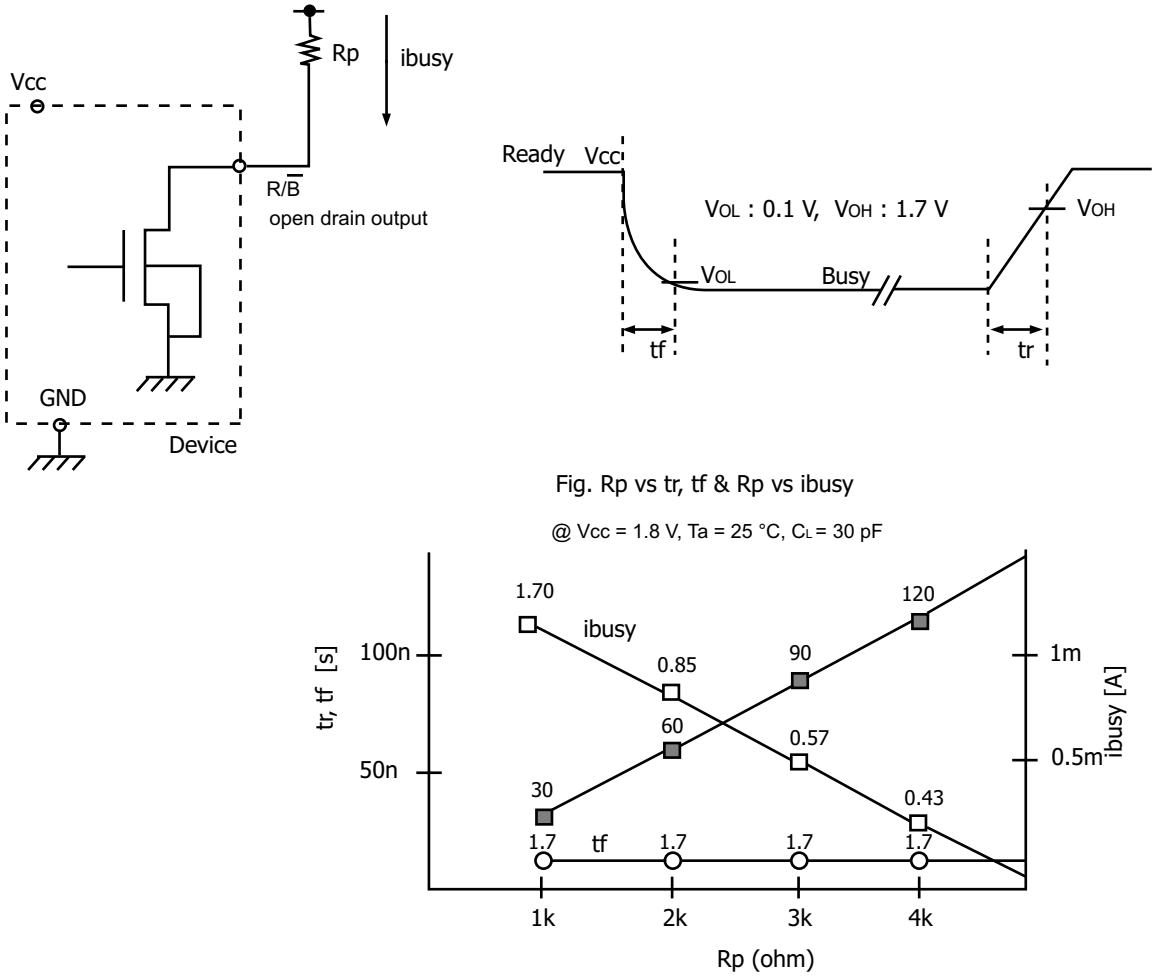



Fig. Rp vs tr, tf & Rp vs ibusy

Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{1.65\ V}{3\ mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

**Figure 18: Ready / Busy Pin Electrical Specifications**

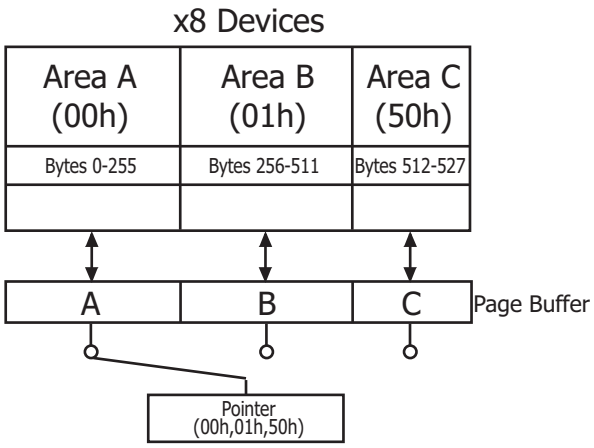



**Figure 19: Pointer Operations**

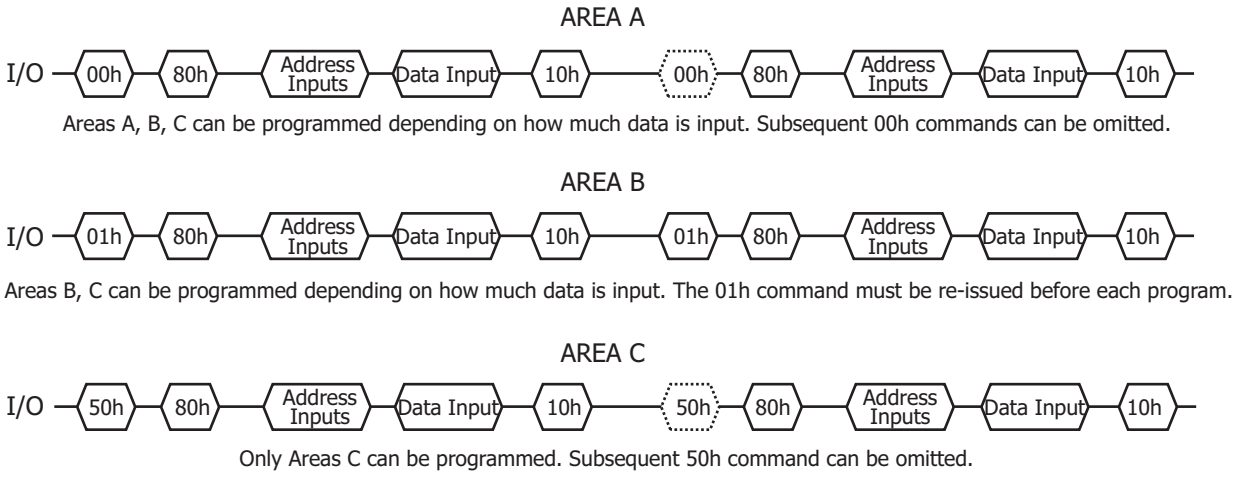



**Figure 20 : Pointer Operation for Programming**

**Bad Block Management**

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 31. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

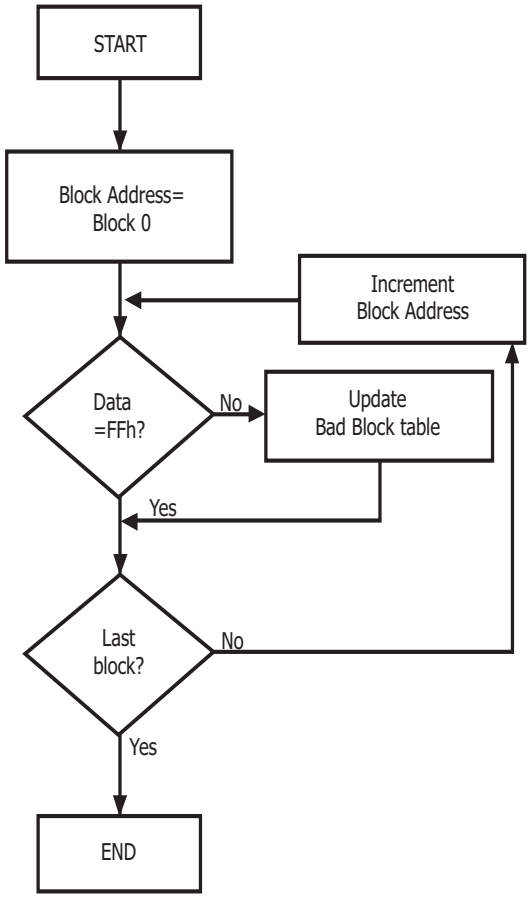



**Figure 21: Bad Block Management Flowchart**

**Block Replacement**

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
The Copy Back Program command can be used to copy the data to a valid block.
*See the "Copy Back Program" section for more details.*
Refer to Table 19 for the recommended procedure to follow if an error occurs during an operation.

| Operation | Recommended Procedure |
|---|---|
| Erase | Block Replacement |
| Program | Block Replacement or ECC (with 1bit/528byte) |
| Read | ECC (with 1bit/528byte) |

**Table 17 : Block Failure**

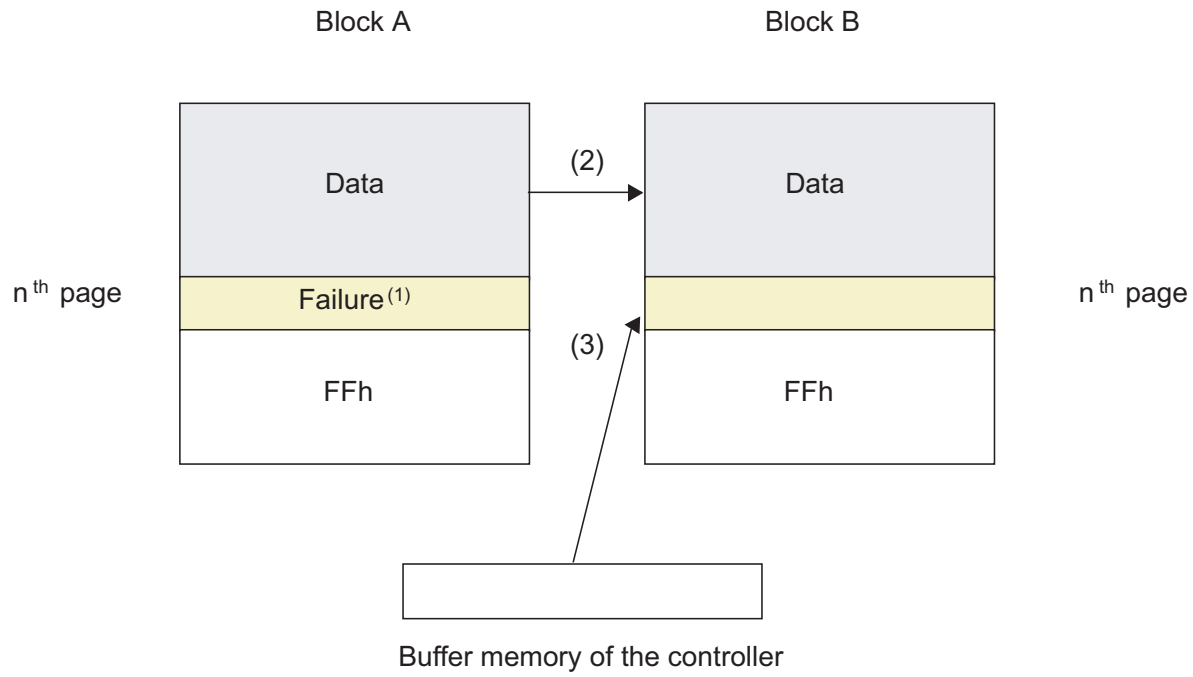



**Figure 22 : Bad Block Replacement**

**NOTE :**
1. An error occurs on $n^{th}$ page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. $N^{th}$ data of block A which is in controller buffer memory is copied into $n^{th}$ page of Block B.
4. Bad block table should be updated to prevent from eraseing or programming Block A.

## Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low ($t_{WW}$ = 100ns, min). The operations are enabled and disabled as follows (Figure 23~26)

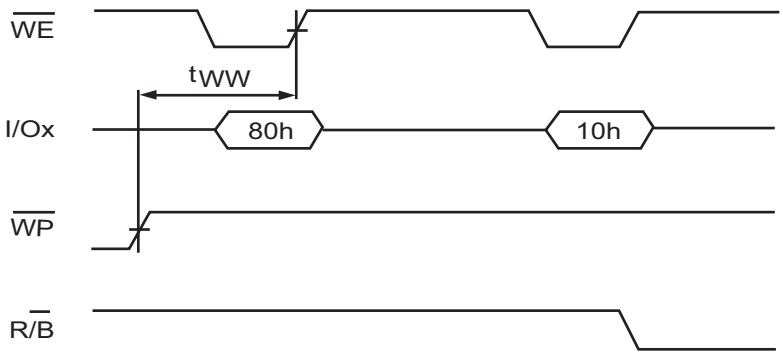



**Figure 23 : Enable Programming**

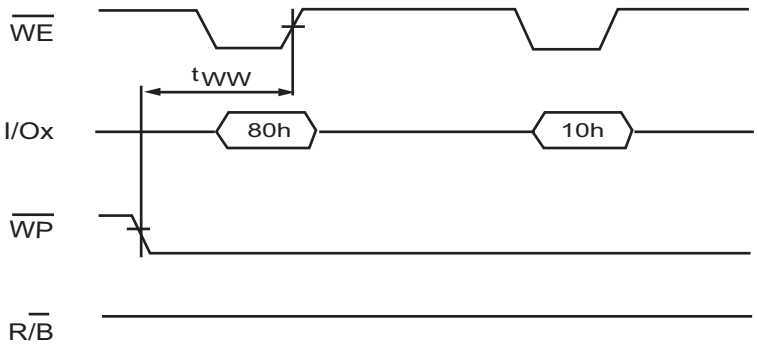



**Figure 24 : Disable Programming**

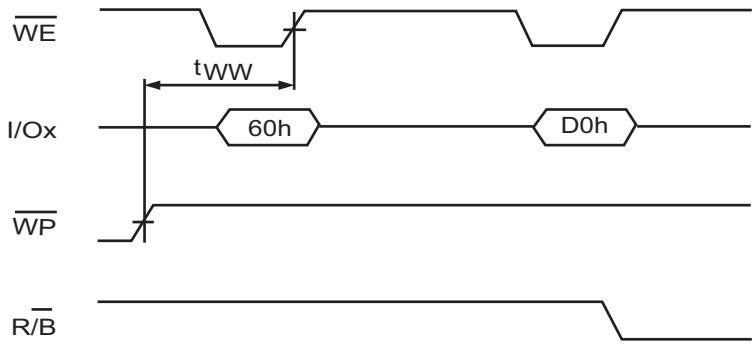



**Figure 25: Enable Erasing**

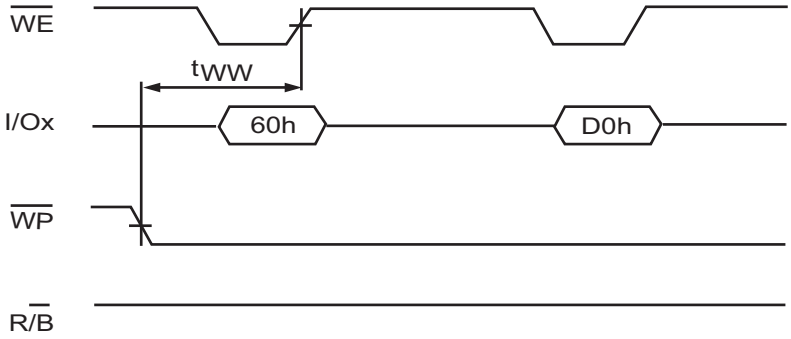



**Figure 26: Disable Erasing**

# 512Mb (16Mbx32) Mobile SDR D-Die

# DESCRIPTION

The Hynix Mobile SDR DRAM is suited for non-PC application which use the batteries such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, handheld PCs.
The Hynix 512M Mobile SDRAM is 536,870,912-bit CMOS Mobile Synchronous DRAM(Mobile SDR), ideally suited for the main memory applications which requires large memory density and high bandwidth. It is organized as 4banks of 4,194,304x32.

The Hynix Mobile SDR DRAM is a type of DRAM which operates in synchronization with input clock. The Hynix Mobile SDRAM latch each control signal at the rising edge of a basic input clock (CLK) and input/output data in synchronization with the input clock (CLK). The address lines are multiplexed with the Data Input/ Output signals on a multiplexed x32 Input/ Output bus. All the commands are latched in synchronization with the rising edge of CLK.

The Hynix Mobile SDR DRAM provides for programmable read or write Burst length of Programmable burst lengths: 1, 2, 4, 8 locations or full page. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. The Mobile SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compartible with the *2n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, randon-access operation.

Read and write accesses to the the Hynix Mobile SDR DRAMs are burst oriented;
accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access. A burst of Read or Write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst Read or Write command on any cycle(This pipelined design is not restricted by a *2N* rule).

The Hynix Mobile SDR DRAM also provides for special programmable options including Partial Array Self Refresh of full array, half array, quarter array Temperature Compensated Self Refresh of 45 or 85 degrees $^{o}$C.

The Hynix Mobile SDR DRAM has the special Low Power function of Auto TCSR(Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implanted, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

All inputs are LV-CMOS compatible. Devices will have a $V_{DD}$ and $V_{DDQ}$ supply of 1.8V (nominal).

## BALL DESCRIPTION

| SYMBOL | TYPE | DESCRIPTION |
|---|---|---|
| CLK | INPUT | Clock : The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK |
| CKE | INPUT | Clock Enable : Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh |
| $\overline{CS}$ | INPUT | Chip Select : Enables or disables all inputs except CLK, CKE, DQM0~DQM3 |
| BA0, BA1 | INPUT | Bank Address : Selects bank to be activated during $\overline{RAS}$ activity<br>Selects bank to be read/written during $\overline{CAS}$ activity |
| A0 ~ A12 | INPUT | Row Address : RA0 ~ RA12, Column Address : CA0 ~ CA8<br>Auto-precharge flag : A10 |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | INPUT | Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation<br>Refer function truth table for details |
| DQM0 ~ DQM3 | INPUT | Data Mask:Controls output buffers in read mode and masks input data in write mode |
| DQ0 ~ DQ31 | I/O | Data Input/Output:Multiplexed data input/output pin |
| VDD/VSS | SUPPLY | Power supply for internal circuits |
| VDDQ/VSSQ | SUPPLY | Power supply for output buffers |
| NC | - | No connection |

## ABSOLUTE MAXIMUM RATING

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Ambient Temperature | TA | -30 ~ 85 | °C |
| Storage Temperature | TSTG | -55 ~ 125 | °C |
| Voltage on Any Pin relative to VSS | VIN, VOUT | -1.0 ~ 2.6 | V |
| Voltage on VDD relative to VSS | VDD | -1.0 ~ 2.6 | V |
| Voltage on VDDQ relative to VSS | VDDQ | -1.0 ~ 2.6 | V |
| Short Circuit Output Current | IOS | 50 | mA |
| Power Dissipation | PD | 1 | W |
| Soldering Temperature · Time | TSOLDER | 260 · 20 | °C · Sec |

## DC OPERATING CONDITION (TA= -30 to 85°C )

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VDD | 1.7 | 1.8 | 1.95 | V | 1 |
| Power Supply Voltage | VDDQ | 1.7 | 1.8 | 1.95 | V | 1, 2 |
| Input High Voltage | VIH | 0.8*VDDQ | - | VDDQ+0.3 | V | 1, 2 |
| Input Low Voltage | VIL | -0.3 | - | 0.3 | V | 1, 2 |

**Note :**
1. All Voltages are referenced to VSS = 0V
2. VDDQ must not exceed the level of VDD

## AC OPERATING TEST CONDITION (TA= -30 to 85 °C, VDD = 1.8V, VSS = 0V)

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| AC Input High/Low Level Voltage | VIH / VIL | 0.9*VDDQ/0.2 | V | |
| Input Timing Measurement Reference Level Voltage | Vtrip | 0.5*VDDQ | V | |
| Input Rise/Fall Time | tR / tF | 1 | ns | |
| Output Timing Measurement Reference Level Voltage | Voutref | 0.5*VDDQ | V | |
| Output Load Capacitance for Access Time Measurement | CL | 30 | pF | |

## CAPACITANCE (TA= 25 °C, f=1MHz)

| Parameter | Pin | Symbol | 6/H | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Input capacitance | CLK | CI1 | 2 | 4.0 | pF |
| | A0~A12, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM0~3 | CI2 | 2 | 4.0 | pF |
| Data input/output capacitance | DQ0 ~ DQ31 | CI/O | 2 | 4.5 | pF |

## DC CHARACTERRISTICS I (TA= -30 to 85°C)

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Leakage Current | ILI | -1 | 1 | uA | 1 |
| Output Leakage Current | ILO | -1 | 1 | uA | 2 |
| Output High Voltage | VOH | VDDQ-0.2 | - | V | 3 |
| Output Low Voltage | VOL | - | 0.2 | V | 4 |

**Note :**

1. VIN = 0 to 1.8V. All other pins are not tested under VIN=0V.

2. DOUT is disabled. VOUT= 0 to 1.95V.

3. IOUT = - 0.1mA

4. IOUT = + 0.1mA

## DC CHARACTERISTICS II (TA= -30 to 85°C)

| Parameter | Symbol | Test Condition | Speed | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | 166MHz | 133MHz | 105MHz | | |
| Operating Current | IDD1 | Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA | 60 | 45 | 45 | mA | 1 |
| Precharge Standby Current in Power Down Mode | IDD2P | CKE ≤ VIL(max), tCK = 15ns | 0.3 | | | mA | |
| | IDD2PS | CKE ≤ VIL(max), tCK = ∞ | 0.3 | | | mA | |
| Precharge Standby Current in Non Power Down Mode | IDD2N | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 2clks.<br>All other pins ≥ VDD-0.2V or ≤ 0.2V | 5 | | | mA | |
| | IDD2NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable. | 1 | | | | |
| Active Standby Current in Power Down Mode | IDD3P | CKE ≤ VIL(max), tCK = 15ns | 5 | | | mA | |
| | IDD3PS | CKE ≤ VIL(max), tCK = ∞ | 3 | | | | |
| Active Standby Current in Non Power Down Mode | IDD3N | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 2clks.<br>All other pins ≥ VDD-0.2V or ≤ 0.2V | 10 | | | mA | |
| | IDD3NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable. | 5 | | | | |
| Burst Mode Operating Current | IDD4 | tCK ≥ tCK(min), IOL=0mA<br>All banks active | 70 | 60 | 60 | mA | 1 |
| Auto Refresh Current | IDD5 | tRFC ≥ tRFC(min) | 90 | | | mA | |
| Self Refresh Current | IDD6 | CKE ≤ 0.2V | See Next Page | | | mA | 2 |

**Notes :**

1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open

2. See the tables of next page for more specific IDD6 current values.

## DC CHARACTERISTICS III - Low Power (IDD6)

| Temp. ( °C) | Memory Array | | | Unit |
|---|---|---|---|---|
| | 4 Banks | 2 Banks | 1 Bank | |
| 45 | 250 | 220 | 200 | uA |
| 85 | 500 | 400 | 350 | uA |

1. VDD / VDDQ = 1.8V
2. Related numerical values in this 45°C are examples for reference sample value only.
3. With a on-chip temperature sensor of Mobile memory, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to ambient temperature variations.

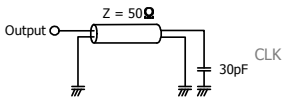
## AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | 166MHz | | 133MHz | | 105MHz | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| System Clock Cycle Time | CAS Latency=3 | tCK3 | 6.0 | 1000 | 7.5 | 1000 | 9.5 | 1000 | ns | |
| | CAS Latency=2 | tCK2 | 12 | 1000 | 12 | 1000 | 15 | 1000 | ns | |
| Clock High Pulse Width | | tCHW | 2.0 | - | 2.5 | - | 3.0 | - | ns | 1 |
| Clock Low Pulse Width | | tCLW | 2.0 | - | 2.5 | - | 3.0 | - | ns | 1 |
| Access Time From Clock | CAS Latency=3 | tAC3 | - | 5.4 | - | 6.0 | - | 7.0 | ns | 2, 3 |
| | CAS Latency=2 | tAC2 | - | 6.0 | - | 8.0 | - | 10 | ns | 2, 3 |
| Data-out Hold Time | | tOH | 2.6 | - | 2.6 | - | 2.6 | - | ns | 3 |
| Data-Input Setup Time | | tDS | 2.0 | - | 2.0 | - | 3.0 | - | ns | 1 |
| Data-Input Hold Time | | tDH | 1.0 | - | 1.0 | - | 1.5 | - | ns | 1 |
| Address Setup Time | | tAS | 2.0 | - | 2.0 | - | 3.0 | - | ns | 1 |
| Address Hold Time | | tAH | 1.0 | - | 1.0 | - | 1.5 | - | ns | 1 |
| CKE Setup Time | | tCKS | 2.0 | - | 2.0 | - | 3.0 | - | ns | 1 |
| CKE Hold Time | | tCKH | 1.0 | - | 1.0 | - | 1.5 | - | ns | 1 |
| Command Setup Time | | tCS | 2.0 | - | 2.0 | - | 3.0 | - | ns | 1 |
| Command Hold Time | | tCH | 1.0 | - | 1.0 | - | 1.5 | - | ns | 1 |
| CLK to Data Output in Low-Z Time | | tOLZ | 1.0 | - | 1.0 | - | 1.0 | - | ns | |
| CLK to Data Output in High-Z Time | CAS Latency=3 | tOHZ3 | | 5.4 | | 6.0 | | 7.0 | ns | |
| | CAS Latency=2 | tOHZ2 | | 6.0 | | 8.0 | | 10 | ns | |

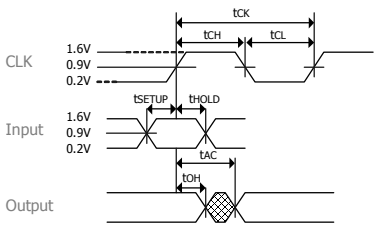
**Notes :**

1. Assume tR / tF (input rise and fall time) is 1ns. If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter.
3. Output Load : 30pF+No termination

- AC high level input voltage / low level input voltage : 1.6 / 0.2V
- Input timing measurement reference level : 0.9V
- Transition time (input rise and fall time) : 0.5ns
- Output timing measurement reference level : 0.9V
- Output load : CL = 30pF



Output Load

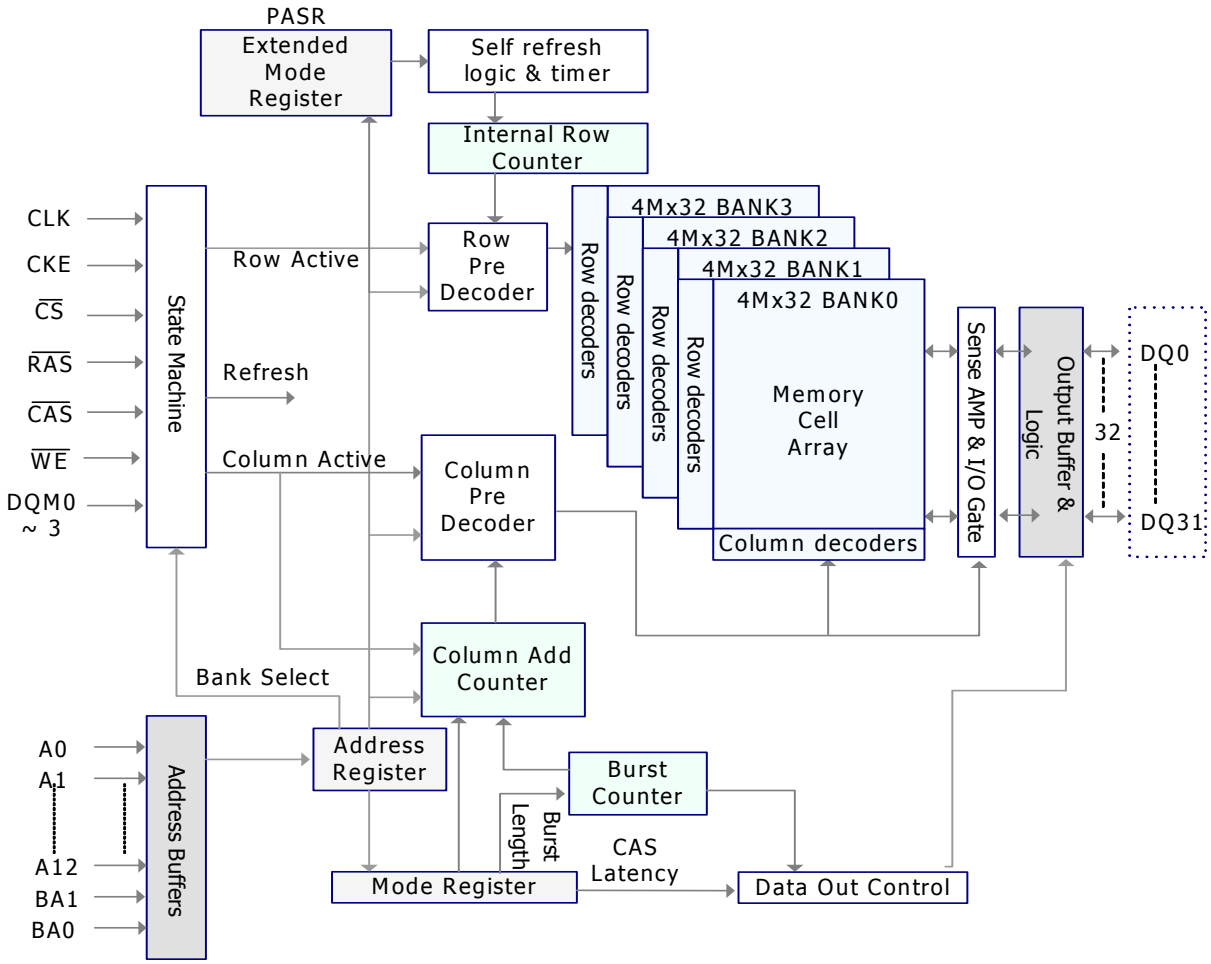


## AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | 166MHz | | 133MHz | | 105MHz | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| $\overline{RAS}$ Cycle Time | | tRC | 60 | - | 72.5 | - | 90 | - | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay | | tRCD | 18 | - | 22.5 | - | 28.5 | - | ns | |
| $\overline{RAS}$ Active Time | | tRAS | 50 | 100K | 50 | 100K | 60 | 100K | ns | |
| $\overline{RAS}$ Precharge Time | | tRP | 18 | - | 22.5 | - | 28.5 | - | ns | |
| $\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay | | tRRD | 12 | - | 15 | - | 19 | - | ns | |
| AUTO REFRESH Period | | tRFC | 80 | - | 80 | - | 80 | - | ns | |
| $\overline{CAS}$ to $\overline{CAS}$ Delay | | tCCD | 1 | - | 1 | - | 1 | - | CLK | |
| Write Command to Data-In Delay | | tWTL | 0 | - | 0 | - | 0 | - | CLK | |
| Data-in to Precharge Command | | tDPL | 2 | - | 2 | - | 2 | - | CLK | |
| Data-In to Active Command | | tDAL | tDPL+tRP | | | | | | | |
| DQM to Data-Out Hi-Z | | tDQZ | 2 | - | 2 | - | 2 | - | CLK | |
| DQM to Data-In Mask | | tDQM | 0 | - | 0 | - | 0 | - | CLK | |
| MRS to New Command | | tMRD | 2 | - | 2 | - | 2 | - | CLK | |
| Precharge to Data Output High-Z | $\overline{CAS}$ Latency=3 | tPROZ3 | 3 | - | 3 | - | 3 | - | CLK | |
| | $\overline{CAS}$ Latency=2 | tPROZ2 | 2 | - | 2 | - | 2 | - | CLK | |
| Power Down Exit Time | | tDPE | 1CLK + tCKS | - | 1CLK + tCKS | - | 1CLK + tCKS | - | CLK | |
| Self Refresh Exit Time | | tXSR | 120 | - | 120 | - | 120 | - | ns | |
| Refresh Time | | tREF | - | 64 | - | 64 | - | 64 | ms | |

# FUNCTIONAL BLOCK DIAGRAM

**4Mbit x 4banks x 32 I/O Mobile Synchronous DRAM**



# BASIC FUNCTIONAL DESCRIPTION

## Mode Register

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | OP Code | 0 | 0 | CAS Latency | | | BT | Burst Length | | |

### OP Code

| A9 | Write Mode |
|---|---|
| 0 | Burst Read and Burst Write |
| 1 | Burst Read and Single Write |

### Burst Type

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

### CAS Latency

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

### Burst Length

| A2 | A1 | A0 | Burst Length | |
|---|---|---|---|---|
| | | | A3 = 0 | A3=1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Full page | Reserved |

## BASIC FUNCTIONAL DESCRIPTION (Continued)

### Extended Mode Register

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DS | | 0 | 0 | PASR | | |

**DS (Driver Strength)**

| A6 | A5 | Driver Strength |
|---|---|---|
| 0 | 0 | Full |
| 0 | 1 | 1/2 Strength |
| 1 | 0 | 1/4 Strength |
| 1 | 1 | Reserved |

**PASR** (Partial Array Self Refresh)

| A2 | A1 | A0 | Self Refresh Coverage |
|---|---|---|---|
| 0 | 0 | 0 | All Banks |
| 0 | 0 | 1 | Half of Total Bank (BA1=0 or Bank 0,1) |
| 0 | 1 | 0 | Quarter of Total Bank (BA1=BA0=0 or Bank 0) |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Half of Bank 0(Bank 0 and Row Address MSB=0) |
| 1 | 1 | 0 | Quarter of Bank 0(Bank 0 and Row Address 2 MSBs=0) |
| 1 | 1 | 1 | Reserved |

## COMMAND TRUTH TABLE

| Function | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | ADDR | A10 /AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | H | X | L | L | L | L | X | Op Code | | | 2 |
| Extended Mode Register Set | H | X | L | L | L | L | X | Op Code | | | 2 |
| No Operation | H | X | L | H | H | H | X | X | | | |
| Device Deselect | H | X | H | X | X | X | X | X | | | |
| Bank Active | H | X | L | L | H | H | X | Row Address | | V | |
| Read | H | X | L | H | L | H | | Column | L | V | |
| Read with Autoprecharge | H | X | L | H | L | H | X | Column | H | V | |
| Write | H | X | L | H | L | L | X | Column | L | V | |
| Write with Autoprecharge | H | X | L | H | L | L | X | Column | H | V | |
| Precharge All Banks | H | X | L | L | H | L | X | X | H | X | |
| Precharge selected Bank | H | X | L | L | H | L | X | X | L | V | |
| Burst stop | H | X | L | H | H | L | X | X | | | |
| Data Write/Output Enable | H | X | X | | | | X | X | | | |
| Data Mask/Output Disable | H | X | X | | | | V | X | | | |
| Auto Refresh | H | H | L | L | L | H | X | X | | | |
| Self Refresh Entry | H | L | L | L | L | H | X | X | | | |
| Self Refresh Exit | L | H | H | X | X | X | X | X | | | 1 |
| | | | L | H | H | H | | | | | |
| Precharge Power Down Entry | H | L | H | X | X | X | X | X | | | |
| | | | L | H | H | H | | | | | |
| Precharge Power Down Exit | L | H | H | X | X | X | X | X | | | |
| | | | L | H | H | H | | | | | |
| Clock Suspend Entry | H | L | H | X | X | X | X | X | | | |
| | | | L | V | V | V | | | | | |
| Clock Suspend Exit | L | H | X | | | | X | X | | | |

**Notes :**

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. BA1/BA0 must be issued 0/0 in the mode register set, and 1/0 in the extended mode register set.

## CURRENT STATE TRUTH TABLE (Sheet 1 of 4)

| Current State | Command | | | | | | | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0/ BA1 | A*max*-A0 | Description | | |
| Idle | L | L | L | L | OP CODE | | Mode Register Set | Set the Mode Register | 14 |
| | L | L | L | H | X | X | Auto or Self Refresh | Start Auto or Self Refresh | 5 |
| | L | L | H | L | BA | X | Precharge | No Operation | |
| | L | L | H | H | BA | Row Add. | Bank Activate | Activate the specified bank and row | |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 4 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 4 |
| | L | H | H | H | X | X | No Operation | No Operation | 3 |
| | H | X | X | X | X | X | Device Deselect | No Operation or Power Down | 3 |
| Row Active | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | Precharge | 7 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | Start Write : optional AP(A10=H) | 6 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | Start Read : optional AP(A10=H) | 6 |
| | L | H | H | H | X | X | No Operation | No Operation | |
| | H | X | X | X | X | X | Device Deselect | No Operation | |
| Read | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | Termination Burst: Start the Precharge | |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | Termination Burst: Start Write(optional AP) | 8,9 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | Termination Burst: Start Read(optional AP) | 8 |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |

## CURRENT STATE TRUTH TABLE (Sheet 2 of 4)

| Current State | Command | | | | | | | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0/ BA1 | A*max*-A0 | Description | | |
| Read | H | X | X | X | X | X | Device Deselect | Continue the Burst | |
| Write | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | Termination Burst: Start the Precharge | 10 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | Termination Burst: Start Write(optional AP) | 8 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | Termination Burst: Start Read(optional AP) | 8,9 |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |
| Read with Auto Precharge | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 4,12 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4,12 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 12 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 12 |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |
| Write with Auto Precharge | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 4,12 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4,12 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 12 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 12 |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |

## CURRENT STATE TRUTH TABLE (Sheet 3 of 4)

| Current State | Command | | | | | | | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0/ BA1 | A*max*-A0 | Description | | |
| Precharging | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | No Operation: Bank(s) idle after tRP | |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4,12 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 4,12 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 4,12 |
| | L | H | H | H | X | X | No Operation | No Operation: Bank(s) idle after tRP | |
| | H | X | X | X | X | X | Device Deselect | No Operation: Bank(s) idle after tRP | |
| Row Activating | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 4,12 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4,11,12 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 4,12 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 4,12 |
| | L | H | H | H | X | X | No Operation | No Operation: Row Active after tRCD | |
| | H | X | X | X | X | X | Device Deselect | No Operation: Row Active after tRCD | |
| Write Recovering | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 4,13 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4,12 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | Start Write: Optional AP(A10=H) | |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | Start Read: Optional AP(A10=H) | 9 |
| | L | H | H | H | X | X | No Operation | No Operation: Row Active after tDPL | |

## CURRENT STATE TRUTH TABLE (Sheet 4 of 4)

| Current State | Command | | | | | | | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0/ BA1 | A*max*-A0 | Description | | |
| Write Recovering | H | X | X | X | X | X | Device Deselect | No Operation: Row Active after tDPL | |
| Write Recovering with Auto Precharge | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 4,13 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 4,12 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 4,12 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 4,9,12 |
| | L | H | H | H | X | X | No Operation | No Operation: Precharge after tDPL | |
| | H | X | X | X | X | X | Device Deselect | No Operation: Precharge after tDPL | |
| Refreshing | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 13 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 13 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 13 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 13 |
| | L | H | H | H | X | X | No Operation | No Operation: idle after tRC | |
| | H | X | X | X | X | X | Device Deselect | No Operation: idle after tRC | |
| Mode Register Accessing | L | L | L | L | OP CODE | | Mode Register Set | ILLEGAL | 13,14 |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | 13 |
| | L | L | H | L | BA | X | Precharge | ILLEGAL | 13 |
| | L | L | H | H | BA | Row Add. | Bank Activate | ILLEGAL | 13 |
| | L | H | L | L | BA | Col Add. A10 | Write/WriteAP | ILLEGAL | 13 |
| | L | H | L | H | BA | Col Add. A10 | Read/ReadAP | ILLEGAL | 13 |
| | L | H | H | H | X | X | No Operation | No Operation: idle after 2 clock cycles | |
| | H | X | X | X | X | X | Device Deselect | No Operation: idle after 2 clock cycles | |

**Notes :**

1. H: Logic High, L: Logic Low, X: Don't care, BA: Bank Address, AP: Auto Precharge.
2. All entries assume that CKE was active during the preceding clock cycle.
3. If both banks are idle and CKE is inactive, then in power down cycle
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address, depending on the state of that bank.
5. If both banks are idle and CKE is inactive, then Self Refresh mode.
6. Illegal if $t_{RCD}$ is not satisfied.
7. Illegal if $t_{RAS}$ is not satisfied.
8. Must satisfy burst interrupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy $t_{DPL}$.
11. Illegal if $t_{RRD}$ is not satisfied
12. Illegal for single bank, but legal for other banks in multi-bank devices.
13. Illegal for all banks.
14. Mode Register Set and Extended Mode Register Set is same command truth table except BA1.

## CKE Enable(CKE) Truth TABLE (Sheet 2 of 1)

| Current State | CKE | | Command | | | | | | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0, BA1 | A*max* -A0 | | |
| Self Refresh | H | X | X | X | X | X | X | X | INVALID | 1 |
| | L | H | H | X | X | X | X | X | Exit Self Refresh with Device Deselect | 2 |
| | L | H | L | H | H | H | X | X | Exit Self Refresh with No Operation | 2 |
| | L | H | L | H | H | L | X | X | ILLEGAL | 2 |
| | L | H | L | H | L | X | X | X | ILLEGAL | 2 |
| | L | H | L | L | X | X | X | X | ILLEGAL | 2 |
| | L | L | X | X | X | X | X | X | Maintain Self Refresh | |
| Power Down | H | X | X | X | X | X | X | X | INVALID | 1 |
| | L | H | H | X | X | X | X | X | Power Down mode exit, all banks idle | 2 |
| | | | L | H | H | H | X | X | | |
| | L | H | L | L | X | X | X | X | ILLEGAL | 2 |
| | | | | X | L | X | X | X | | |
| | | | | X | X | L | X | X | | |
| | L | L | X | X | X | X | X | X | Maintain Power Down Mode | |

## CKE Enable(CKE) Truth TABLE (Sheet 2 of 2)

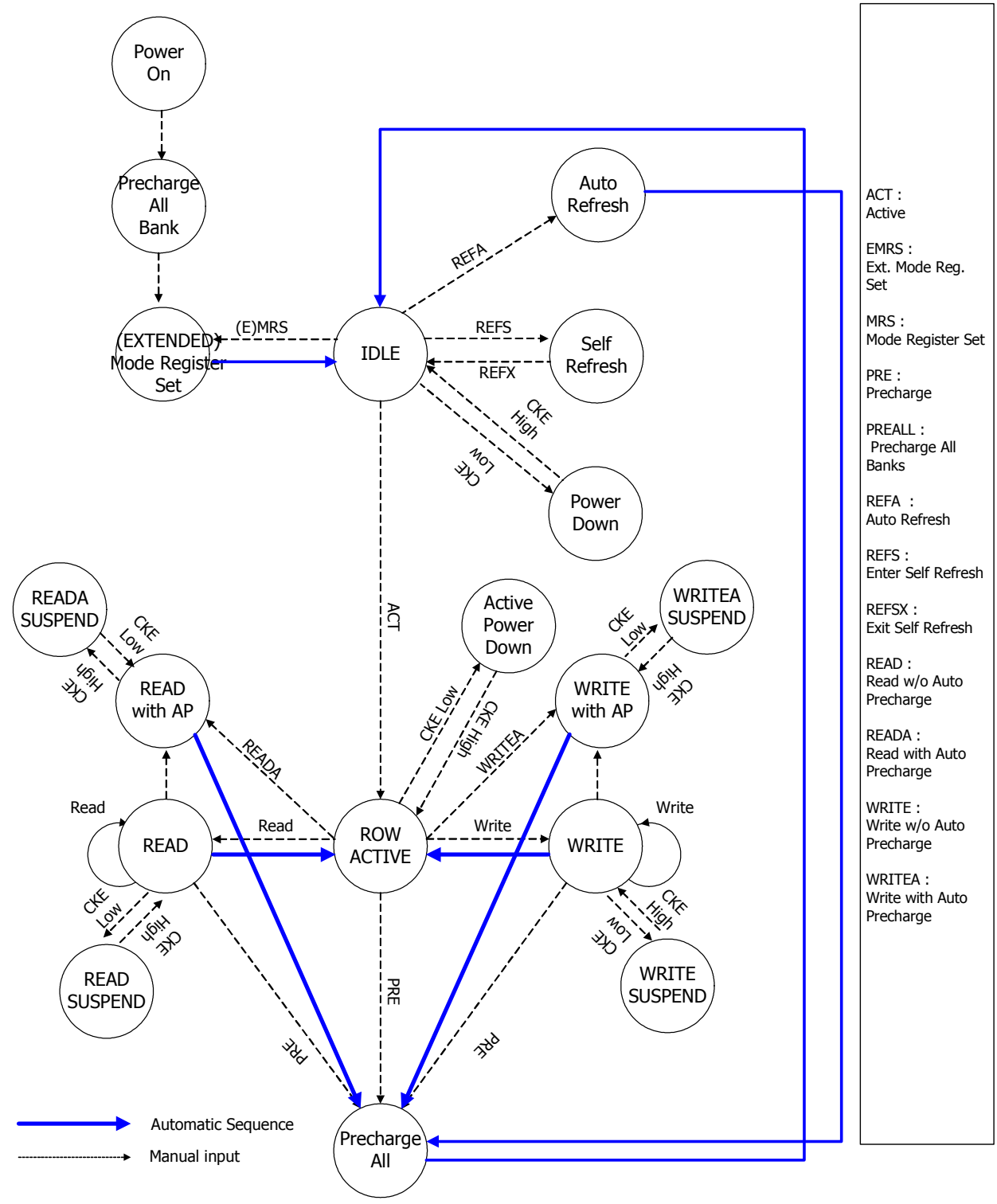
| Current State | CKE | | Command | | | | | | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0, BA1 | A*max*-A0 | | |
| All Banks Idle | H | H | H | X | X | X | | | Refer to the idle State section of the Current State Truth Table | 3 |
| | H | H | L | H | X | X | | | | 3 |
| | H | H | L | L | H | X | | | | 3 |
| | H | H | L | L | L | H | X | X | Auto Refresh | |
| | H | H | L | L | L | L | OP CODE | | Mode Register Set | 4 |
| | H | L | H | X | X | X | | | Refer to the idle State section of the Current State Truth Table | 3 |
| | H | L | L | H | X | X | | | | 3 |
| | H | L | L | L | H | X | | | | 3 |
| | H | L | L | L | L | H | X | X | Entry Self Refresh | 4 |
| | H | L | L | L | L | L | OP CODE | | Mode Register Set | |
| | L | X | X | X | X | X | X | X | Power Down | 4 |
| Any State other than listed above | H | H | X | X | X | X | X | X | Refer to operations of the Current State Truth Table | |
| | H | L | X | X | X | X | X | X | Begin Clock Suspend next cycle | |
| | L | H | X | X | X | X | X | X | Exit Clock Suspend next cycle | |
| | L | L | X | X | X | X | X | X | Maintain Clock Suspend | |

**Notes :**

1. For the given current state CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously.
   When exiting power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high.
3. The address inputs depend on the command that is issued.
4. The Precharge Power Down mode, the Self Refresh mode, and the Mode Register Set can only be entered from the all banks idle state.
5. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously.

## Mobile SDR SDRAM OPERATION

State Diagram



## DESELECT

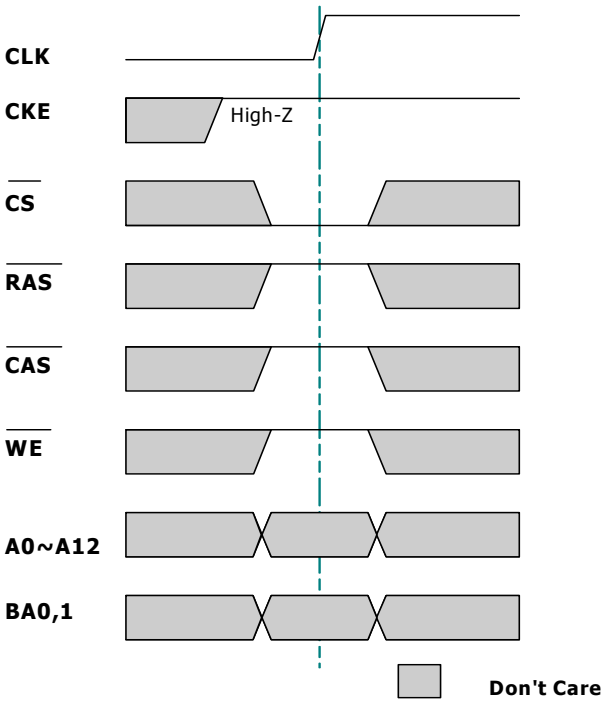
The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the Mobile SDRAM, the Mobile SDRAM ignore command input at the clock. However, the internal status is held. The Mobile SDRAM is effectively deselected. Operations already in progress are not affected.

## NO OPERATION

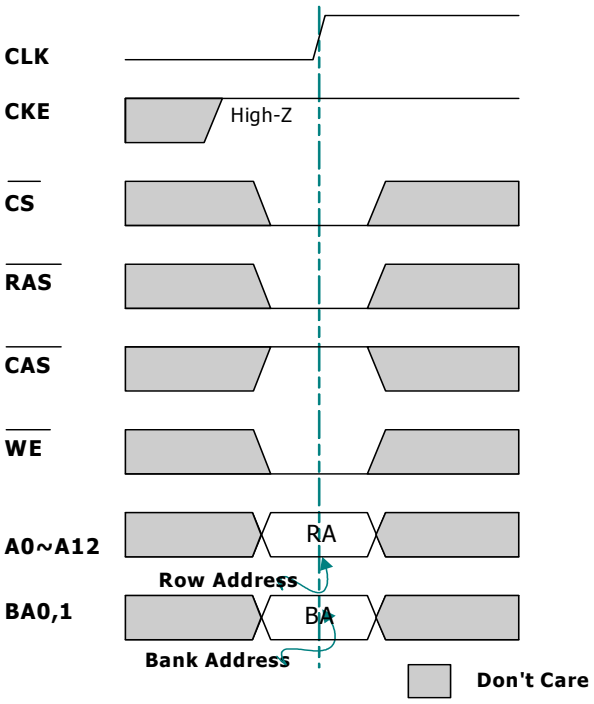
The NO OPERATION (NOP) command is used to perform a NOP to a Mobile SDRAM that is selected ($\overline{CS}$ = Low, $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = High). This command is not an execution command. However, the internal operations continue. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

## ACTIVE

The Active command is used to activate a row in particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A12(or the highest address bit) selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. (see to next figure)




NOP command



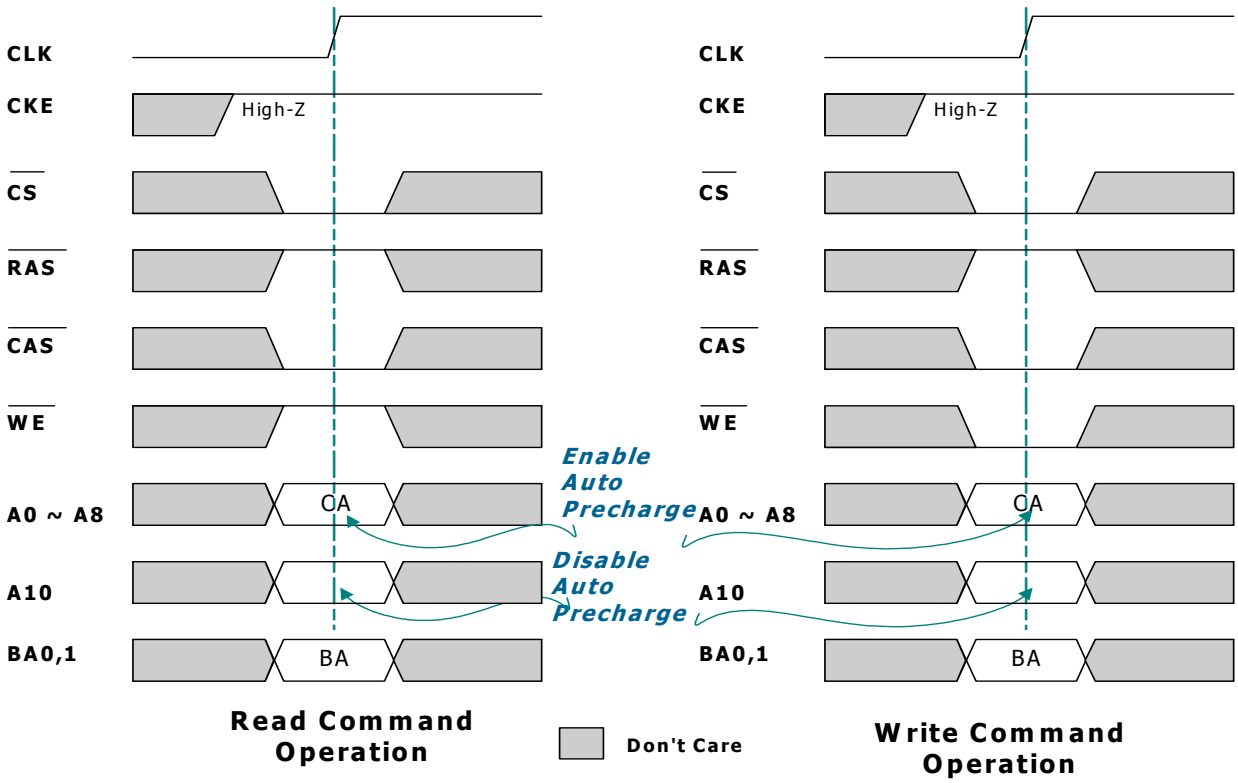

ACTIVATING A SPECIFIC
ROW IN A SPECIFIC BANK

## READ / WRITE COMMAND

Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto-precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued.

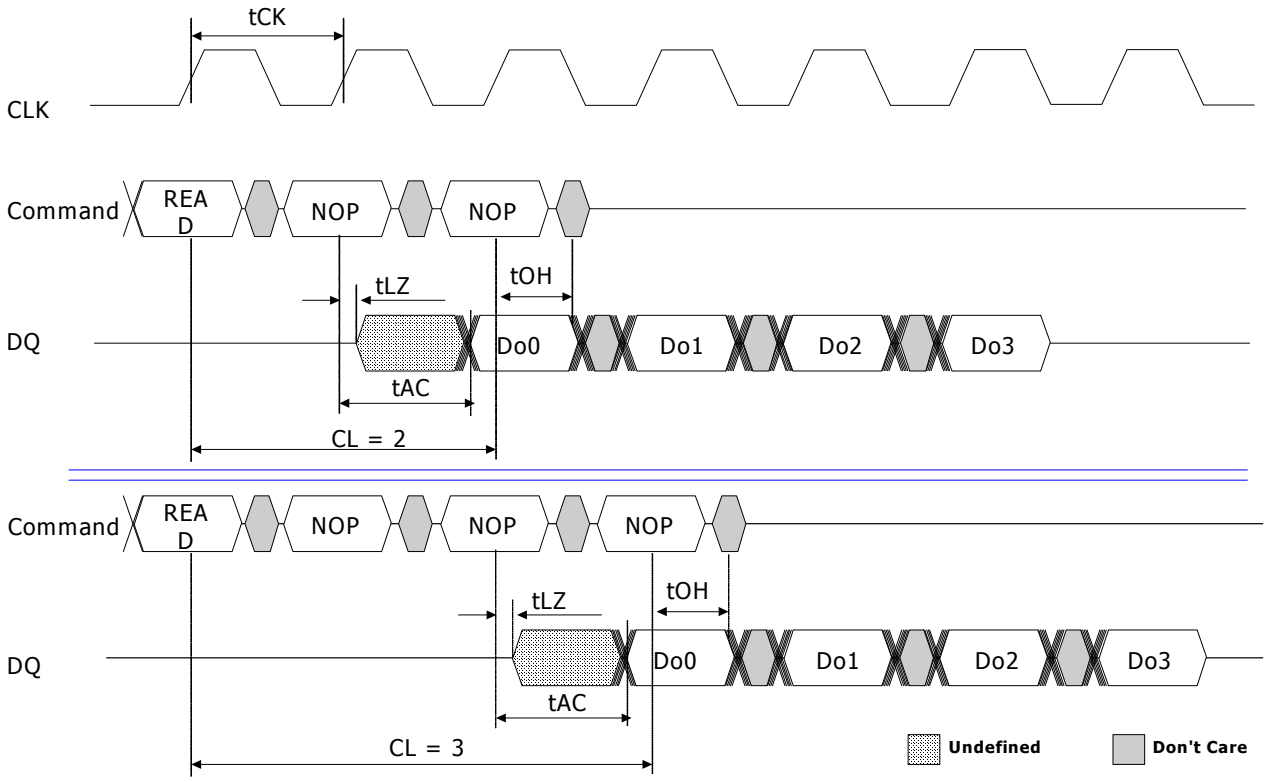
The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto-precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access.




READ / WRITE COMMAND

## READ

A read operation starts when a read command is input. Output buffer becomes Low-Z in the (/CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the /CAS Latency. The /CAS Latency can be set to 2 or 3.
When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.
The /CAS latency and burst length must be specified at the mode register.

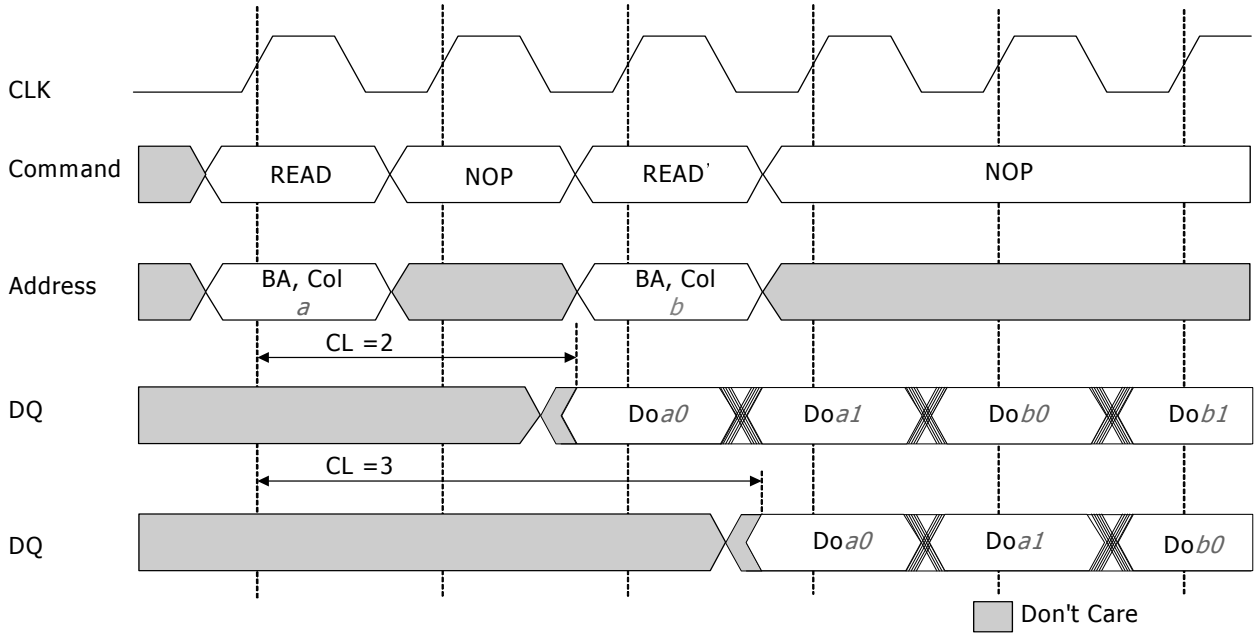



Read Burst Showing CAS Latency

## READ to READ

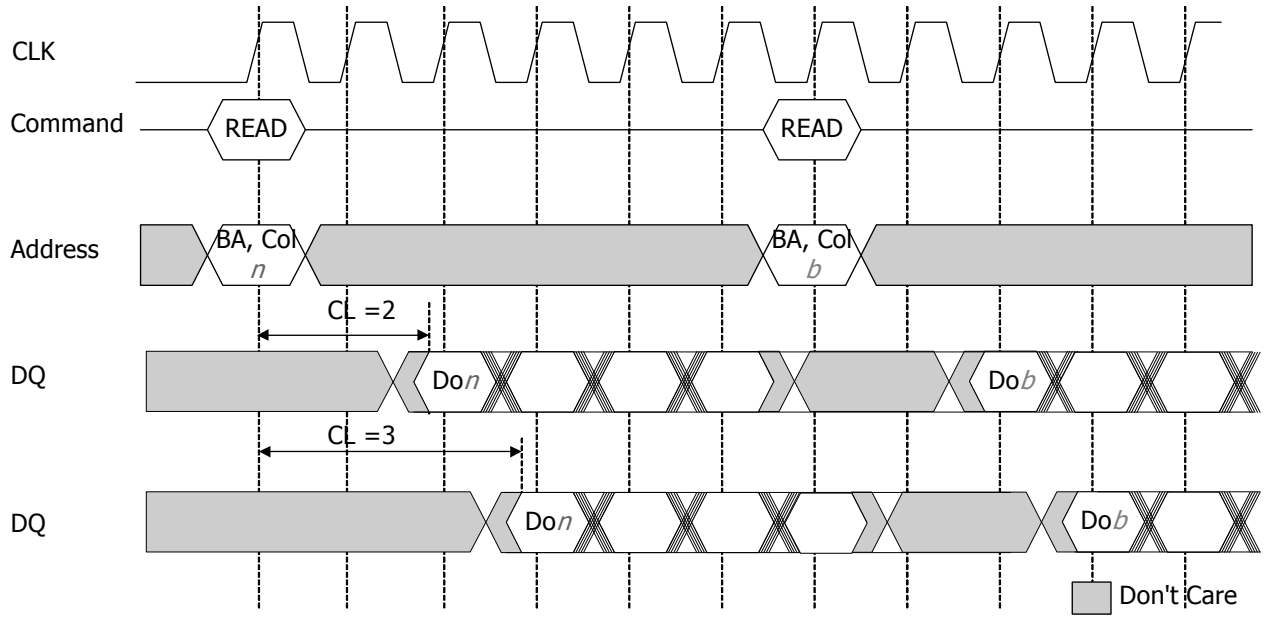
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated.

When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



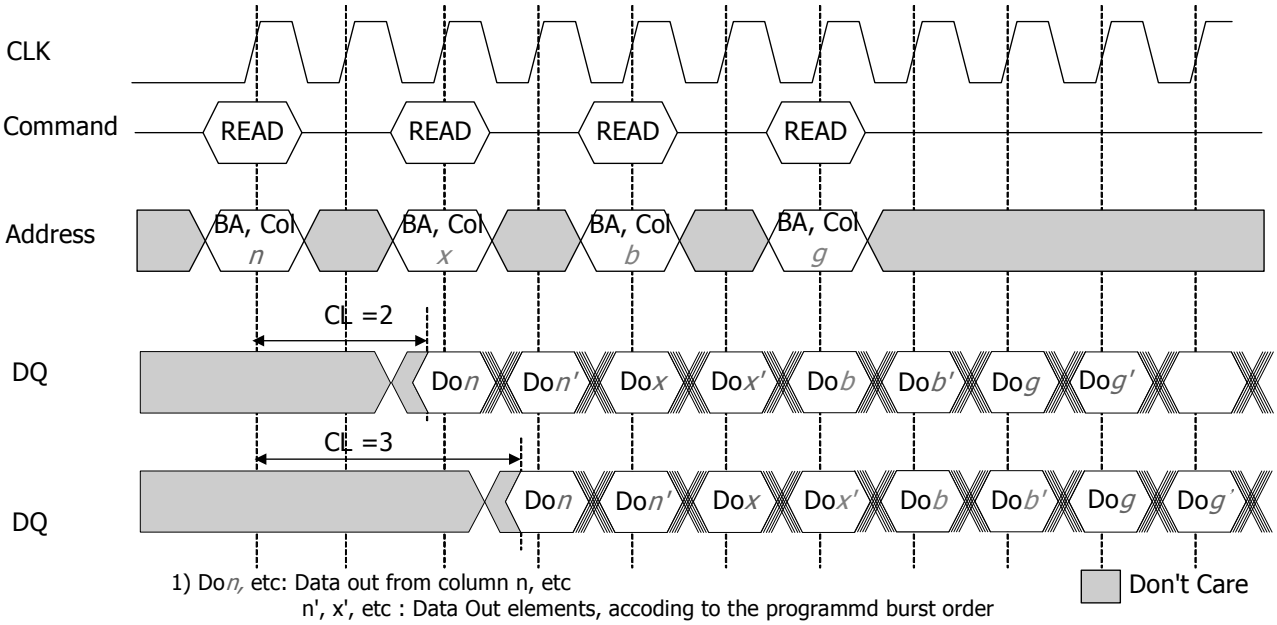

Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in Figure. Full-speed random read accesses within a page or pages can be performed as shown in Fig.




1) Do*n* (or *b*): Data out from column n
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 : 3 subseqnent elements of Data Out appear in the programmed order following Do *n (b)*

Non-Consective Read Bursts

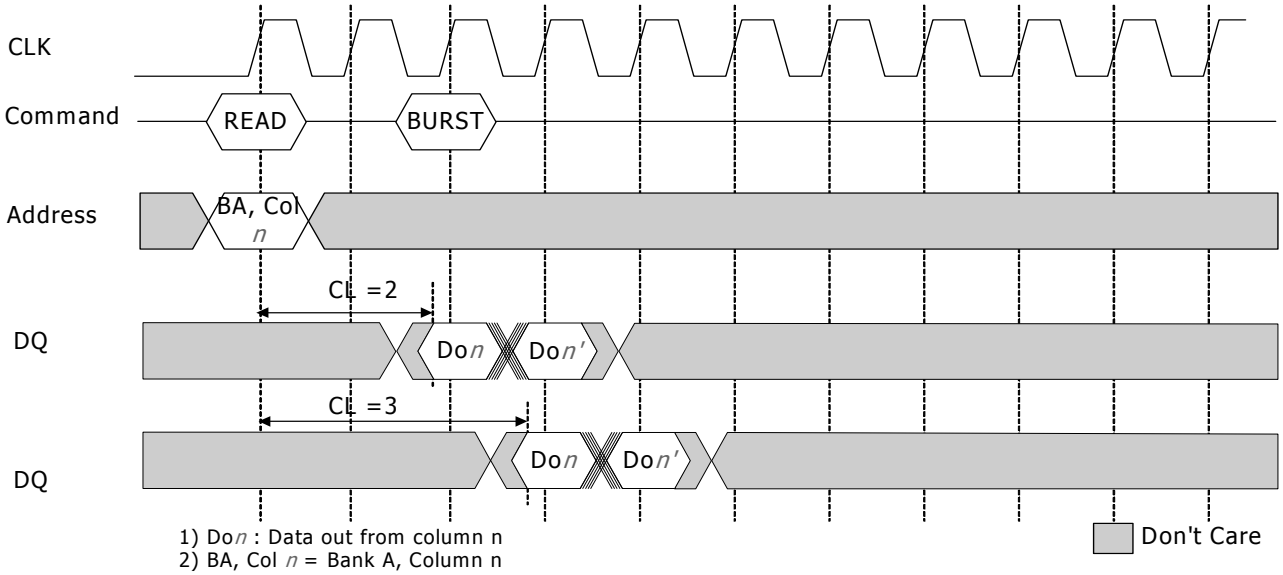



1) Do*n,* etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 1, 2, 4, 8 or full page in cases shown
4) Read are to active row in any banks

Randum Read Bursts

## READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element.

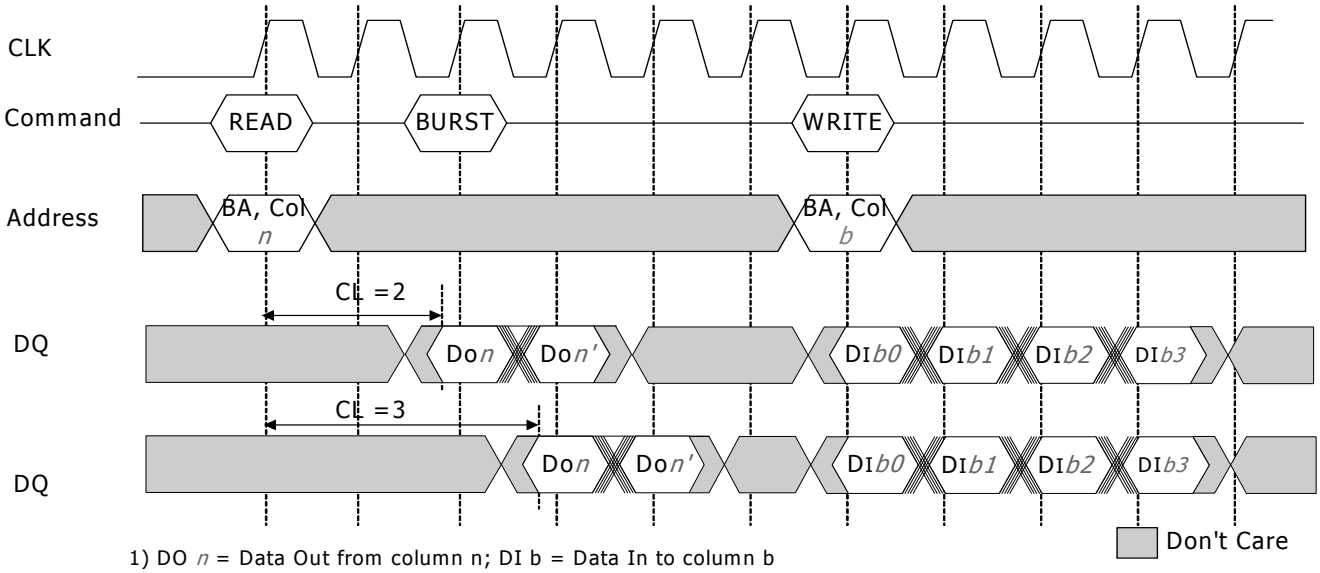



1) Don : Data out from column n
2) BA, Col n = Bank A, Column n
3) Cases shown are bursts of 4, 8, or full page terminated after 2 data elements

Terminating a Read Burst

## READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig.




1) DO *n* = Data Out from column n; DI b = Data In to column b

Read to Write

**Notes :**

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQM must be set High so that the output buffer becomes High-Z before data input.

2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.

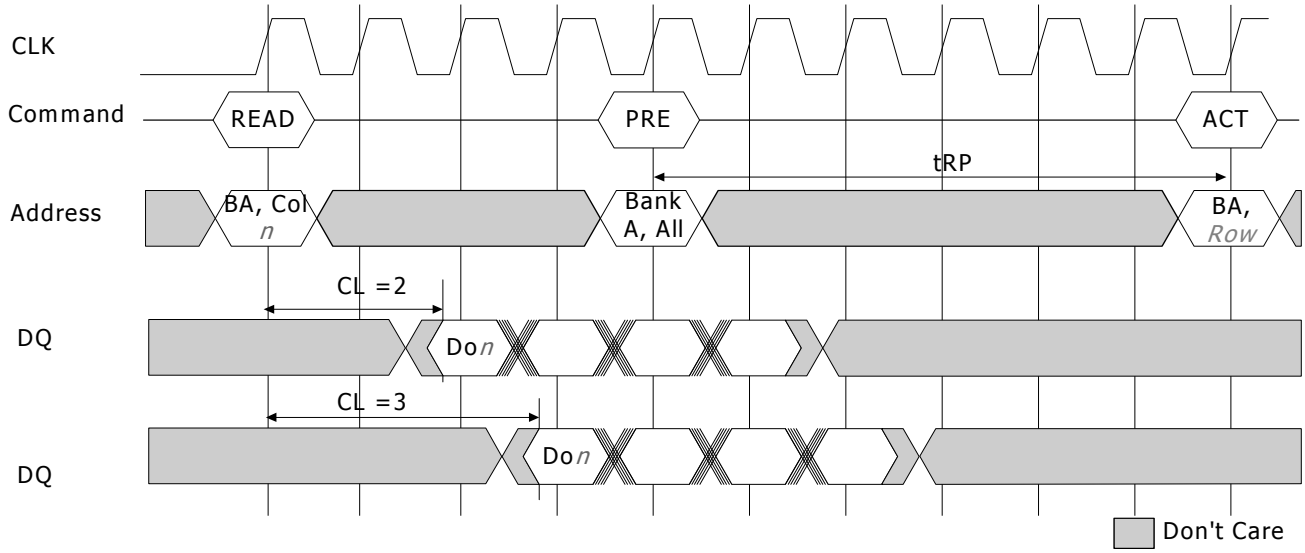
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

## READ to PRECHARGE

Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto pre-charge.

The disadvantage of the PRECHARGEcommand is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to trun-cate fixed-length or full-page bursts.



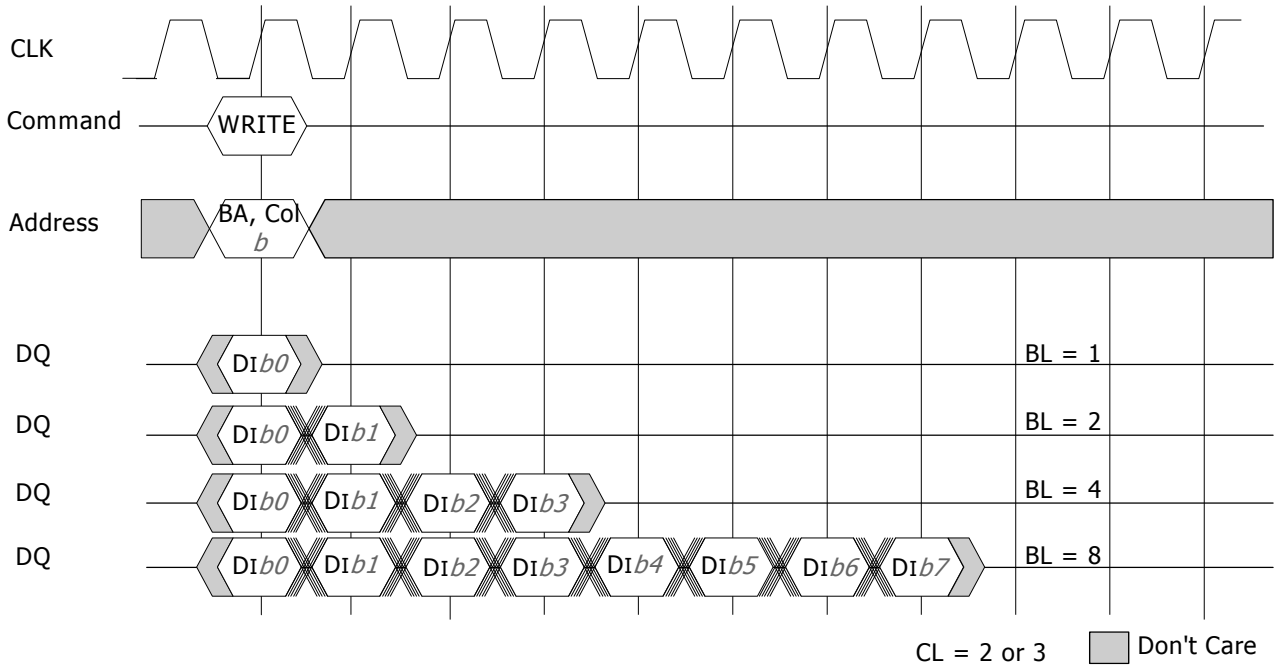

1) DO *n* = Data Out from column n
2) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
3) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

## Write

Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.

During WRITE bursts, the first valild data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored. A full-page burst will continue until terminated.
Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command.



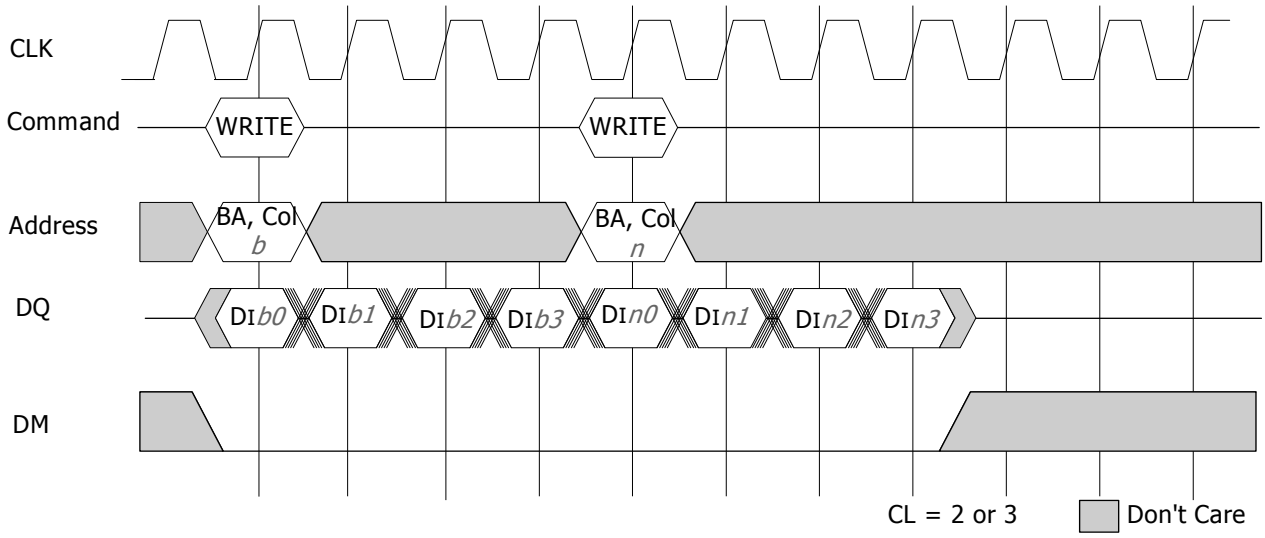

**Basic Write timing parameters for** Write Burst Operation

**Notes :**

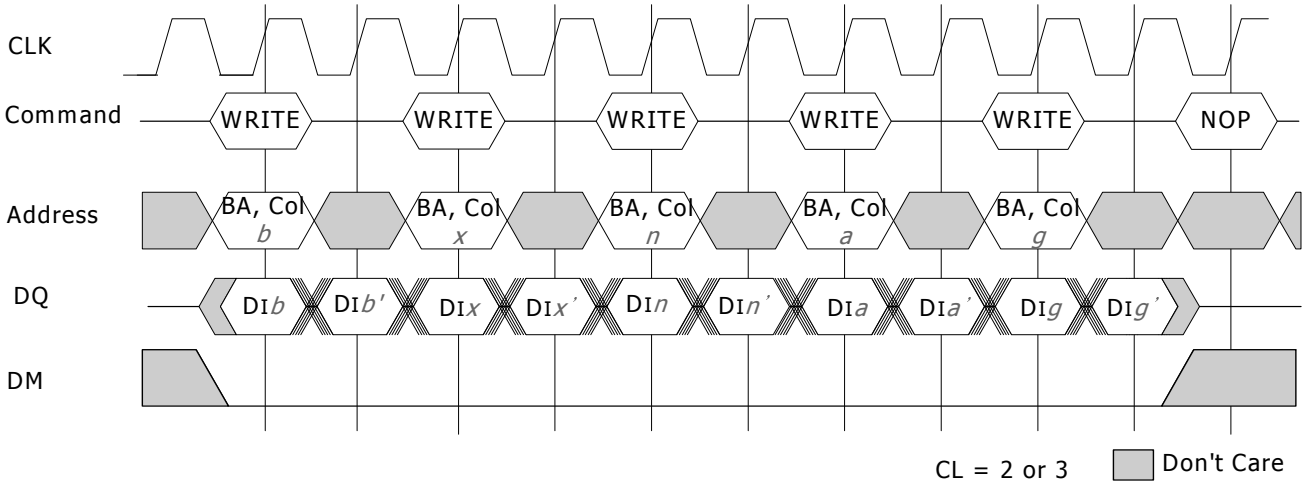
1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.

## WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command. The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element.

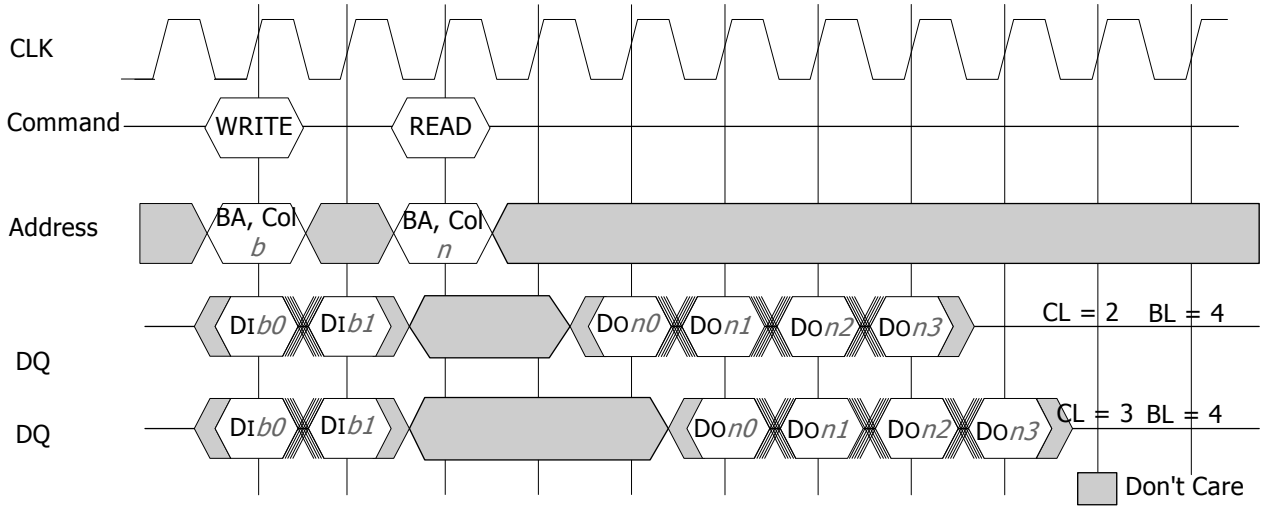



Concatenated Write Bursts




Random Write Cycles

## WRITE to READ




The preceding burst write operation can be aborted and a new burst read operation can be started by inputting a new read command in the write cycle. The data of the read command (READ) is output after the lapse of the /CAS latency.

The preceding write operation (WRIT) writes only the data input before the read command.

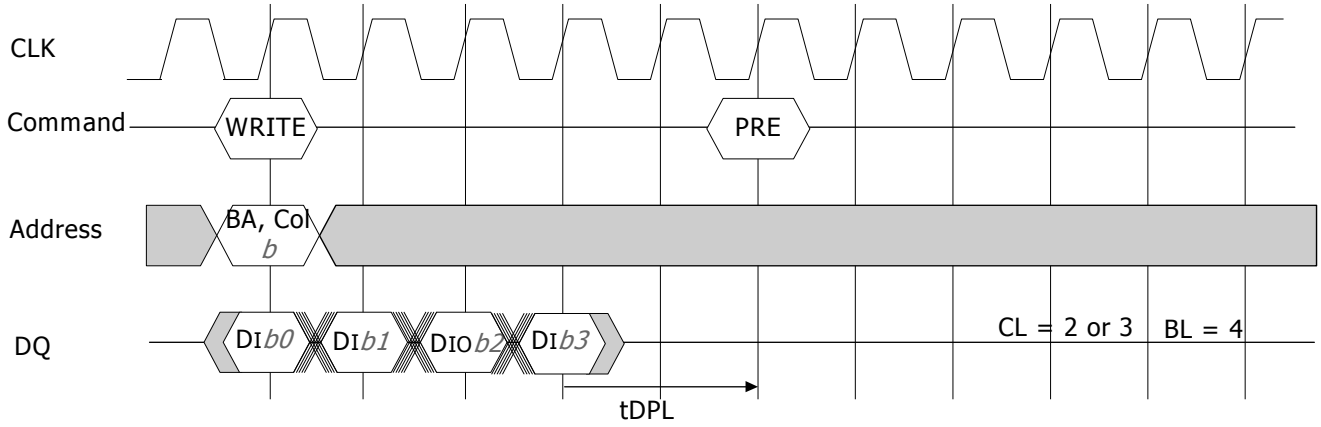
The data bus must go into a high-impedance state at least one cycle before output of the latest data.

**Notes:**

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.
2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

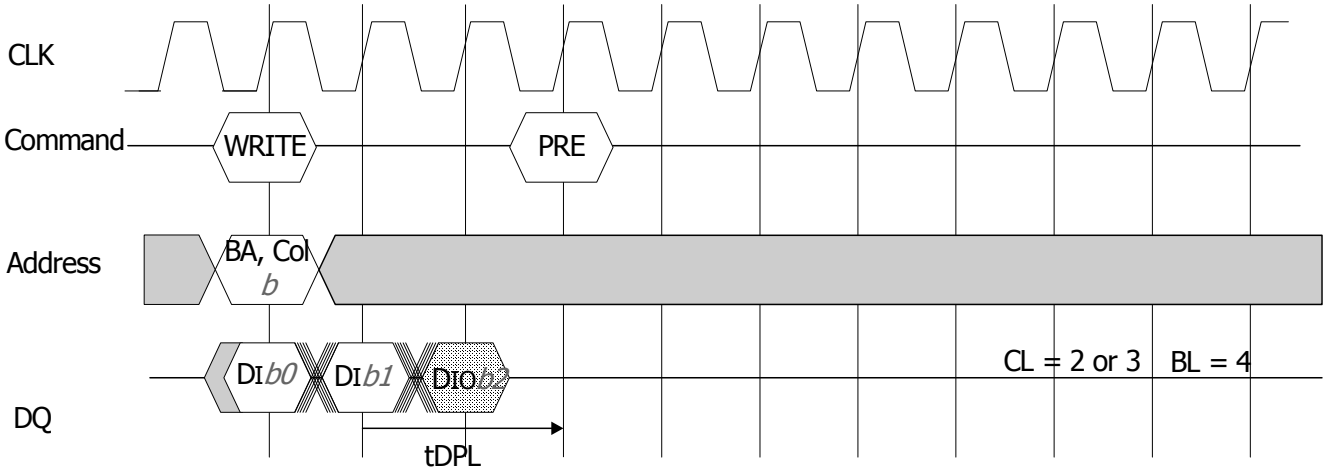
## WRITE to PRECHARGE

Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the clock defined by tDPL. To follow a WRITE without truncating the WRITE burst, tDPL should be met as shown in Fig.




Non-Interrupting Write to Precharge

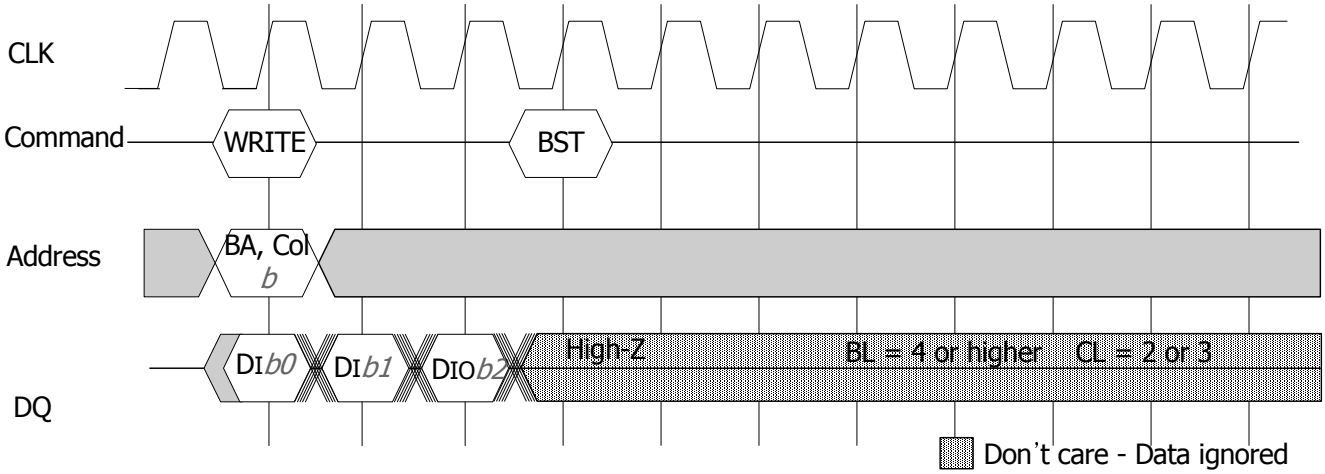
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-inthat are registered prior to the tDPL period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.




Interrupting Write to Precharge

## WRITE BURST TERMINATE

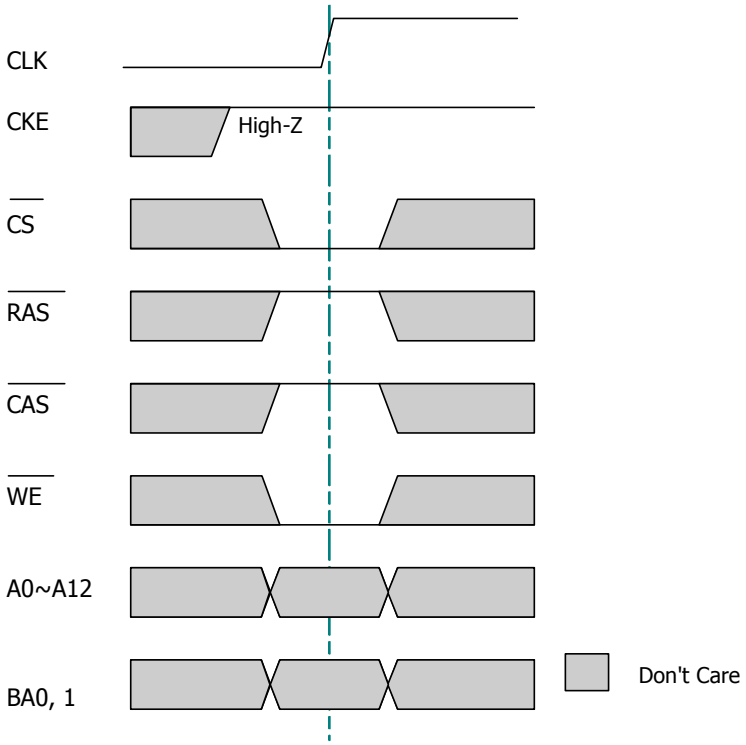
WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command.




Terminating a Burst Write command with BST

## BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

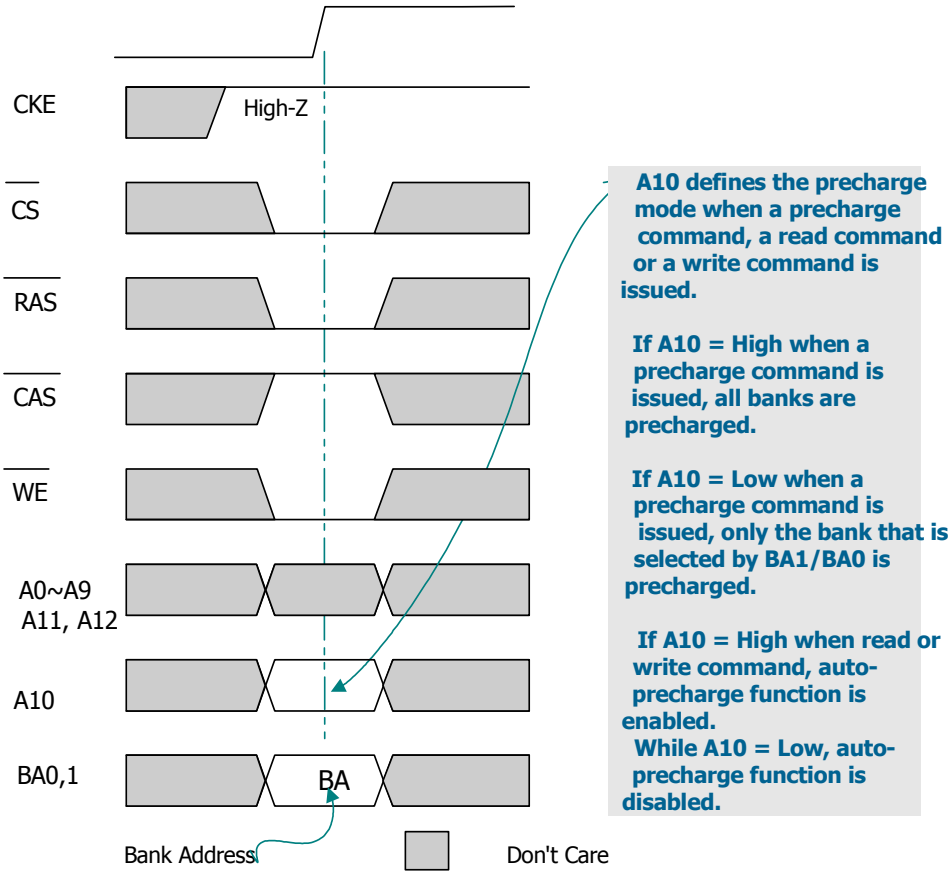



BURST TERMINATE COMMAND

## PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.

If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.




PRECHARGE command

## AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.

This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.

Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed.

## AUTO REFRESH AND SELF REFRESH

Mobile SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

**– AUTO REFRESH.**

This command is used during normal operation of the Mobile SDRAM. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller.The Mobile SDRAM requires AUTO REFRESH commands at an average periodic interval of tREF.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given Mobile SDRMA, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREF.

**-SELF REFRESH.**

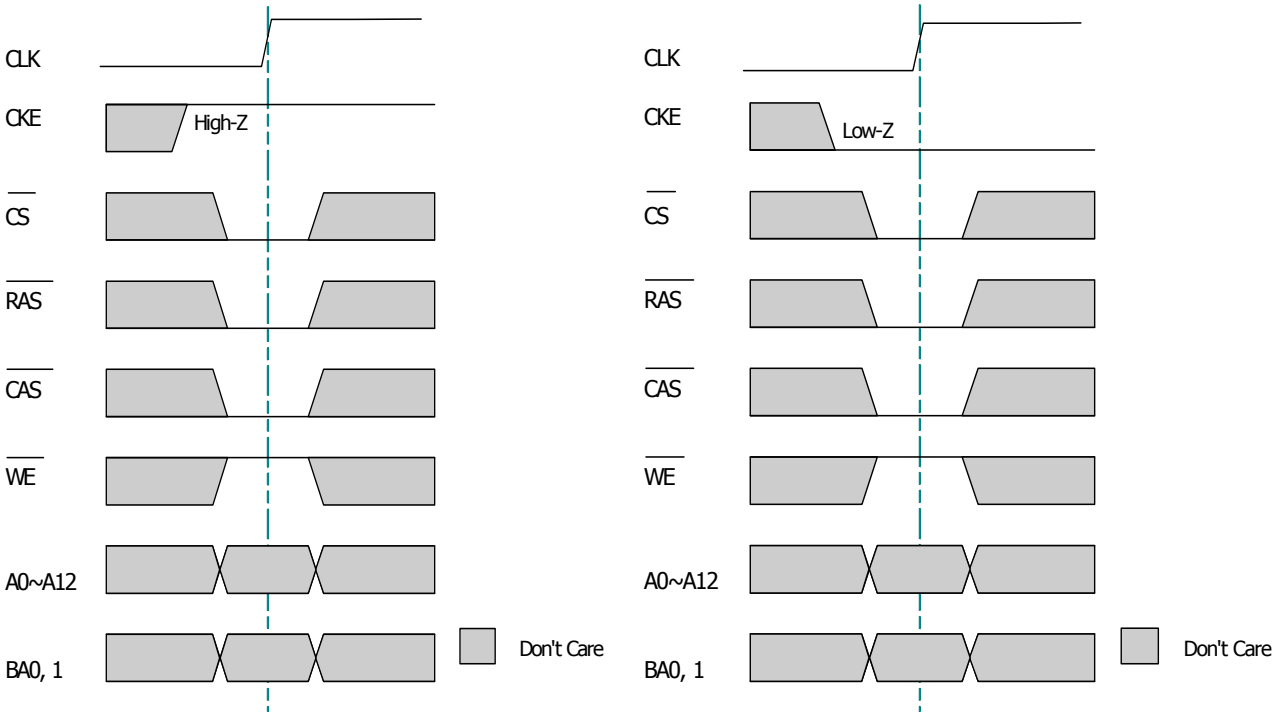
This state retains data in the Mobile SDRAM, even if the rest of the system is powered down. Note refresh interval timing while in Self Refresh mode is scheduled internally in the Mobile SDRAM and may vary and may not meet tREF time. After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During selfrefresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF (max.) period on the condition 1 and 2 below.

1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below*after exiting from self-refresh mode.

**Note:** tREF (max.) / refresh cycles.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. In the self refresh mode, two additional power-saving options exist. They are Temperature Compensated Self Refresh and Partial Array Self Refresh and are described in the Extended Mode Register section.
The Self Refresh command is used to retain cell data in the Mobile SDRAM. In the Self Refresh mode, the Mobile SDRAM operates refresh cycle asynchronously.

The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled(Low). The Mobile SDRAM can accomplish an special Self Refresh operation by the specific modes(PASR) programmed in extended mode registers. The Mobile SDRAM can control the refresh rate automatically by the temperature value of Auto TCSR(Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR(Partial Array Self Refresh). The Mobile SDRAM can reduce the self refresh current(IDD6) by using these two modes.




AUTO REFRESH COMMAND

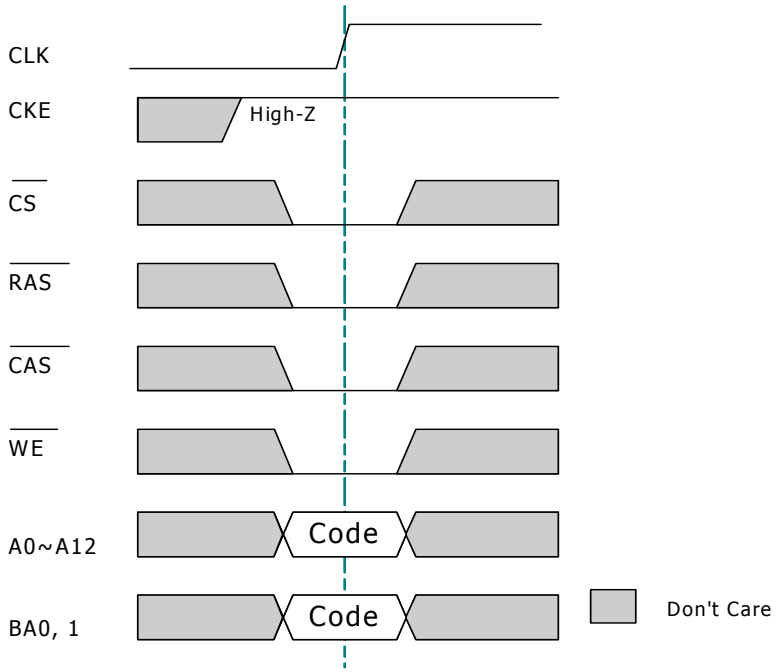
SELF REFRESH ENTRY COMMAND

**Note 1:** If all banks are in the idle status and CKE is inactive (low level), the self refresh mode is set.

| Function | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | ADDR | A10/AP | BA |
|---|---|---|---|---|---|---|---|---|---|---|
| Auto Refresh | H | H | L | L | L | H | X | X | | |
| Self Refresh Entry | H | L | L | L | L | H | X | X | | |

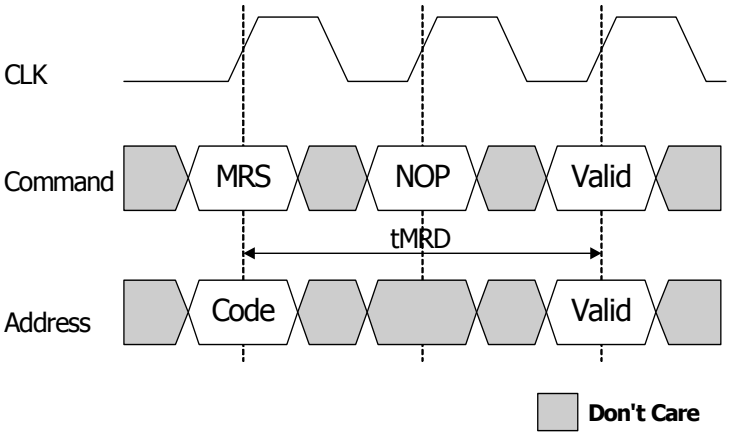
## MODE REGISTER SET

The mode registers are loaded via the address bits.
BA0 and BA1 are used to select between the Mode Register and the Extended Mode Register. See the Mode Register description in the register definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.




MODE REGISTER SET COMMAND

**Note:** BA0=BA1=Low loads the Mode Register, whereas BA0=Low and BA1=High loads the Extended Mode Register.

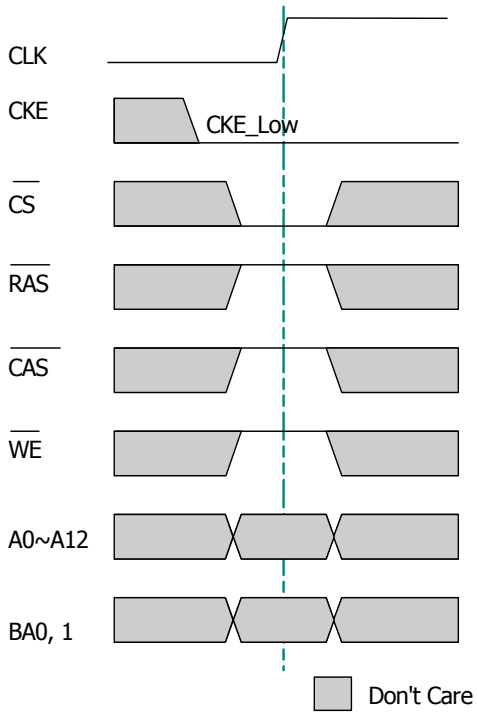



Code = Mode Register / Extended Mode Register selection (BA0, BA1) and op-code (A0 - An)

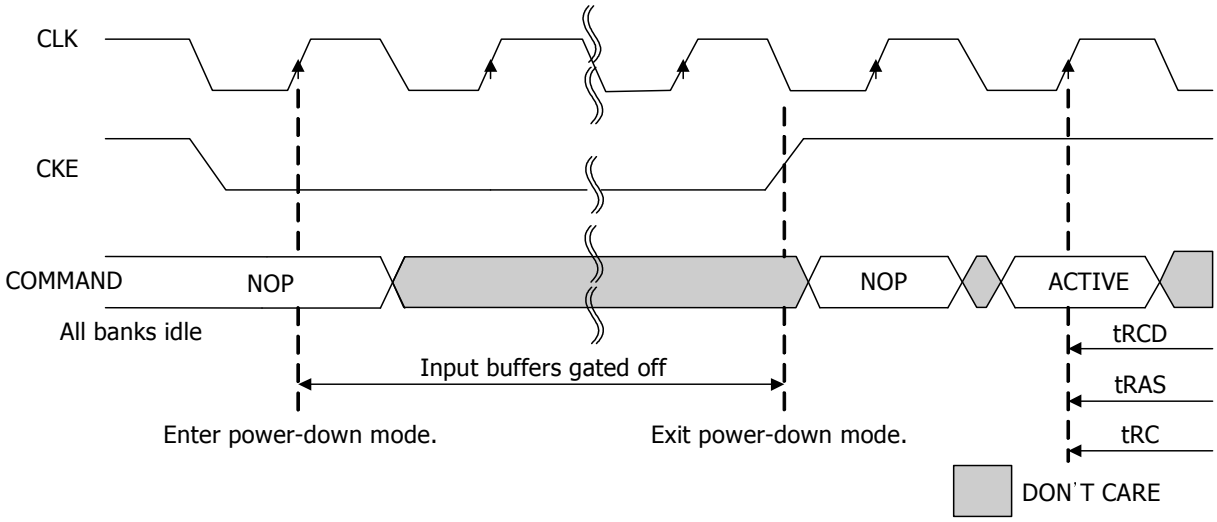
tMRD DEFINITION

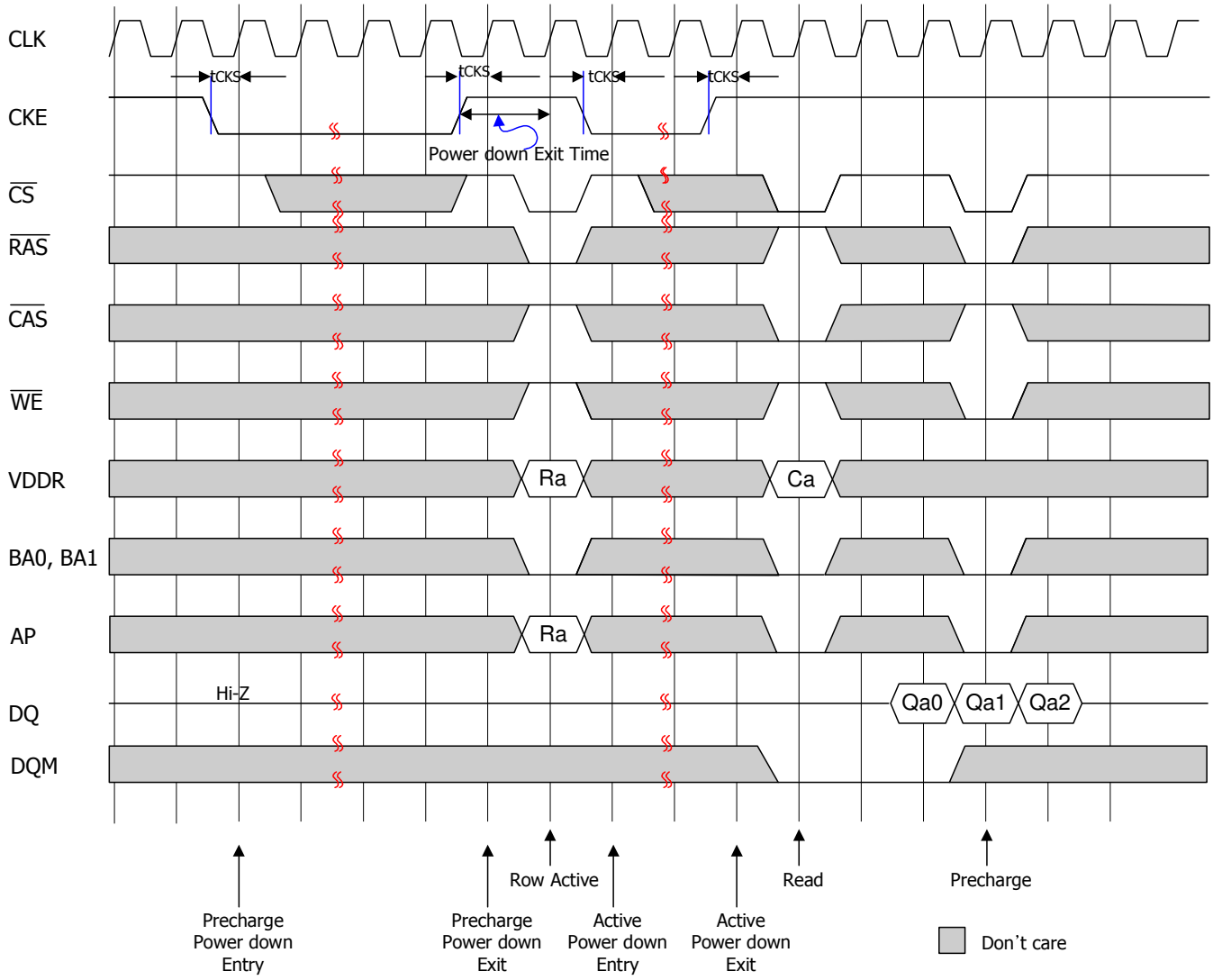
## POWER DOWN

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby.

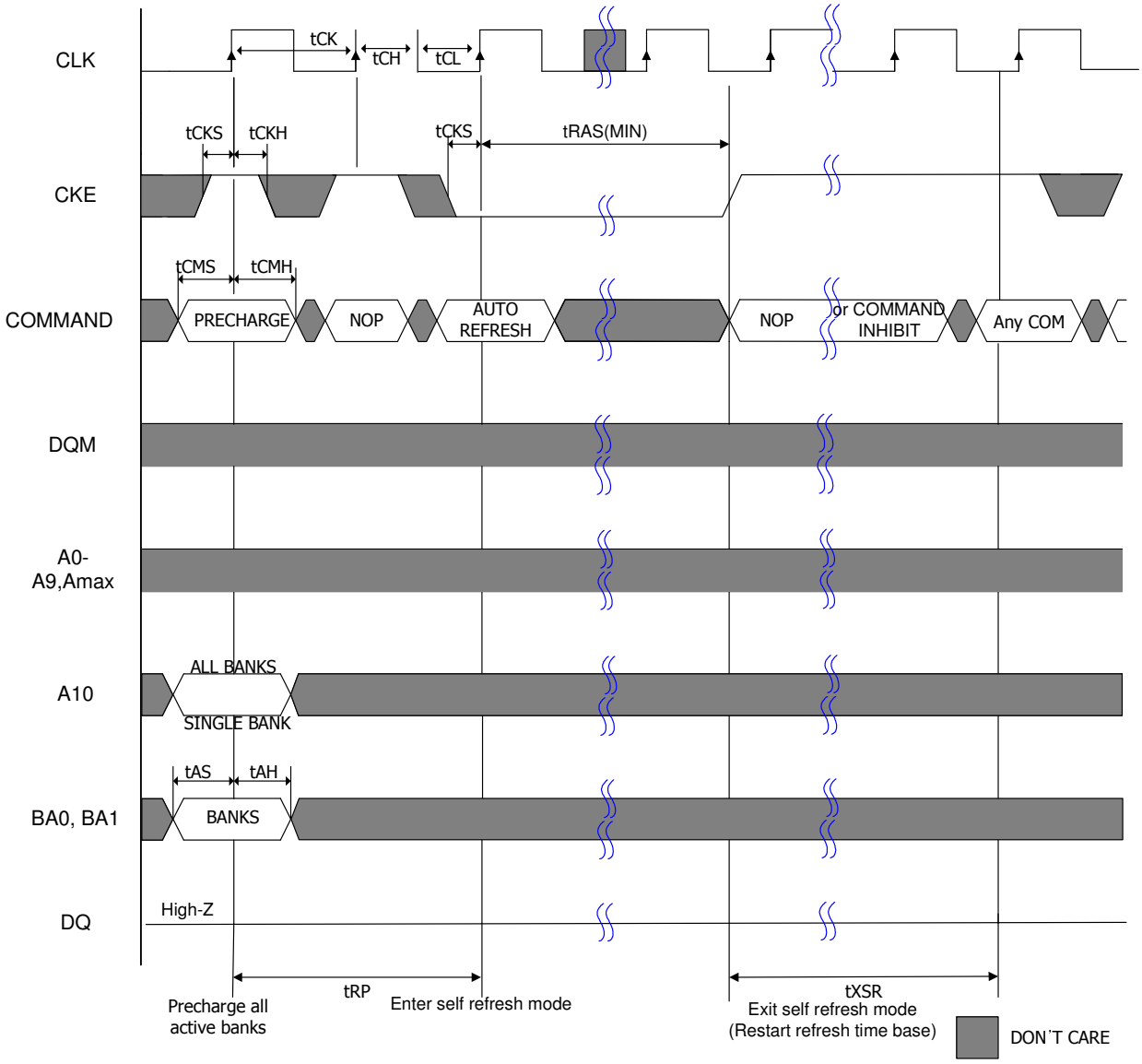



POWER-DOWN COMMAND


CLK
CKE
COMMAND
NOP
NOP
ACTIVE
All banks idle
tRCD
Input buffers gated off
tRAS
tRC
Enter power-down mode.
Exit power-down mode.
DON'T CARE




Note : CKE should be set high at least 1CLK + tCKS prior to Row active command.


CLK
tCK
tCH
tCL
CKE
tCKS
tCKH
tCKS
tRAS(MIN)
COMMAND
tCMS
tCMH
PRECHARGE
NOP
AUTO REFRESH
NOP
or COMMAND INHIBIT
Any COM
DQM
A0-A9,Amax
A10
ALL BANKS
SINGLE BANK
BA0, BA1
tAS
tAH
BANKS
DQ
High-Z
tRP
Precharge all active banks
Enter self refresh mode
tXSR
Exit self refresh mode
(Restart refresh time base)
DON'T CARE

## Power-up and Initialization

Like a Synchronous DRAM, Low Power SDRAM(Mobile SDRAM) must be powered up and initialized in a predefined manner. Power must be applied to VDD and VDDQ(simultaneously). The clock signal must be started at the same time. After power up, an initial pause of 200 usec is required. And a precharge all command will be issued to the Mobile SDRAM. Then, 8 or more Auto refresh cycles will be provided. After the Auto refresh cycles are completed, a mode register set(MRS) command will be issued to program the specific mode of operation (Cas Latency, Burst length, etc.) And a extended mode register set command will be issued to program specific mode of self refresh operation(PASR). The following these cycles, the Mobile SDRAM is ready for normal opeartion.

**Programming the registers**

## Mode Register

The mode register contains the specific mode of operation of the Mobile SDRAM. This register includes the selection of a burst length(1, 2, 4, 8, Full Page), a cas latency(2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.

## Extended Mode Register

The extended mode register contains the specific features of self refresh opeartion of the Mobile SDRAM. This register includes the selection of partial arrays to be refreshed(half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

## Bank(Row) Active

The Bank Active command is used to activate a row in a specified bank of the device. This command is initiated by activating $\overline{CS}$, $\overline{RAS}$ and deasserting $\overline{CAS}$, $\overline{WE}$ at the positive edge of the clock. The value on the BA1 and BA0 selects the bank, and the value on the A0-A12 selects the row. This row remains active for column access until a precharge command is issued to that bank. Read and write opeartions can only be initiated on this activated bank after the minimum $t_{RCD}$ time is passed from the activate command.

## Read

The READ command is used to initiate the burst read of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$, $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A8-A0 address inputs select the sarting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the READ burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.
The length of burst and the CAS latency will be determined by the values programmed during the MRS command.

## Write

The WRITE command is used to initiate the burst write of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ and deasserting $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A8-A0 address inputs select the starting column location. The value on input A10 determines whether or not Auto Precharge is used.
If Auto Precharge is selected the row being accessed will be precharged at the end of the WRITE burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.

## Precharge

The Precharge command is used to close the open row in a particular bank or the open row in all banks. When the precharge command is issued with address A10, high, then all banks will be precharged, and If A10 is low, the open row in a particular bank will be precharged. The bank(s) will be available when the minimum $t_{RP}$ time is met after the precharge command is issued.

## Auto Precharge

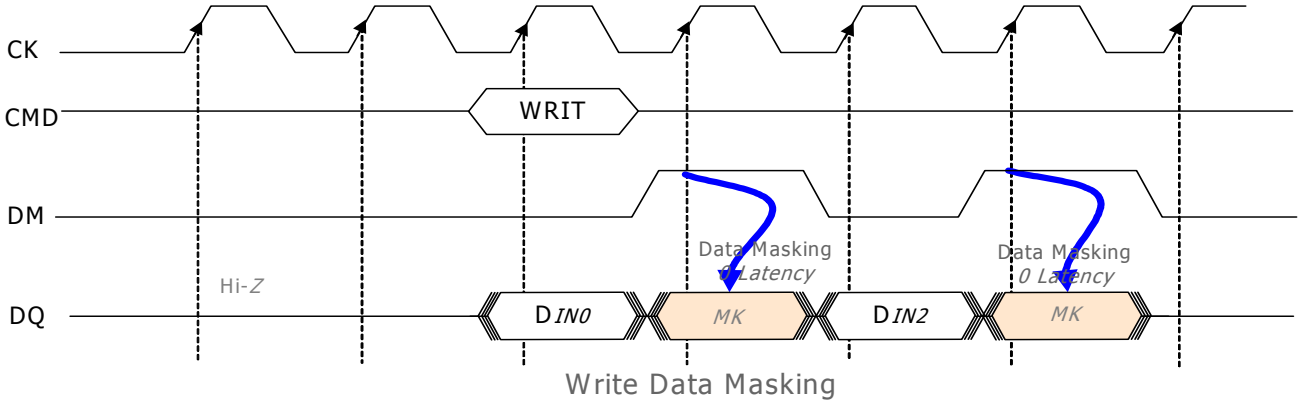
The Auto Precharge command is issued to close the open row in a particular bank after READ or WRITE operation. If A10 is high when a READ or WRITE command is issued, the READ or WRITE with Auto Precharge is initiated.

## Burst Termination

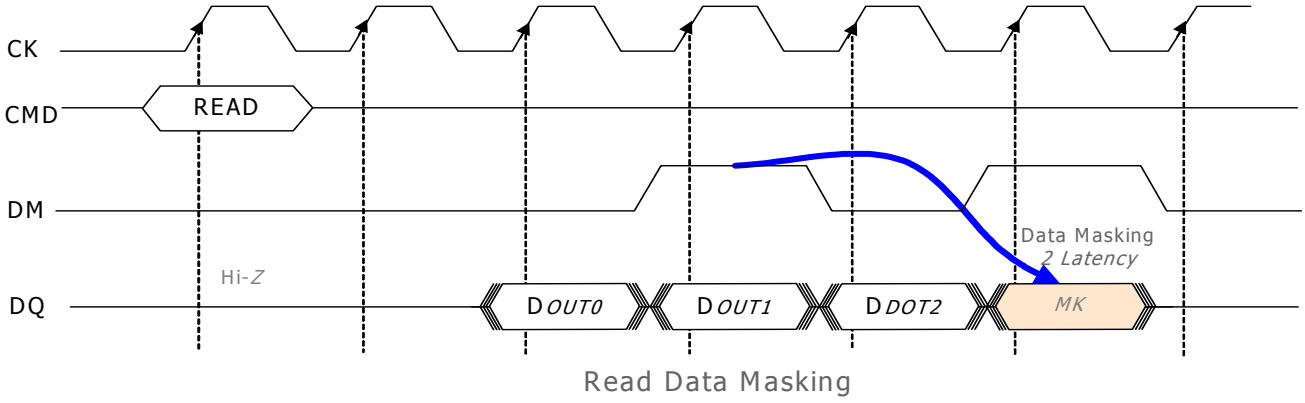
The Burst Termination is used to terminate the burst operation. This function can be accomplished by asserting a Burst Stop command or a Precharge command during a burst READ or WRITE operation. The Precharge command interrupts a burst cycle and close the active bank, and the Burst Stop command terminates the existing burst operation leave the bank open.

## Data Mask

The Data Mask comamnd is used to mask READ or WRITE data. During a READ operation, When this command is issued, data outputs are disabled and become high impedance after two clock delay. During a WRITE operation, When this command is issued, data inputs can't be written with no clock delay.
If data mask is initiated by asserting low on DQM during the read cycle, the data outputs are enabled.
If DQM is asserted to High. the data outputs are masked (disabled) and become Hi-Z state after 2 cycle later. During the write cycle, DQM mask data input with zero latency



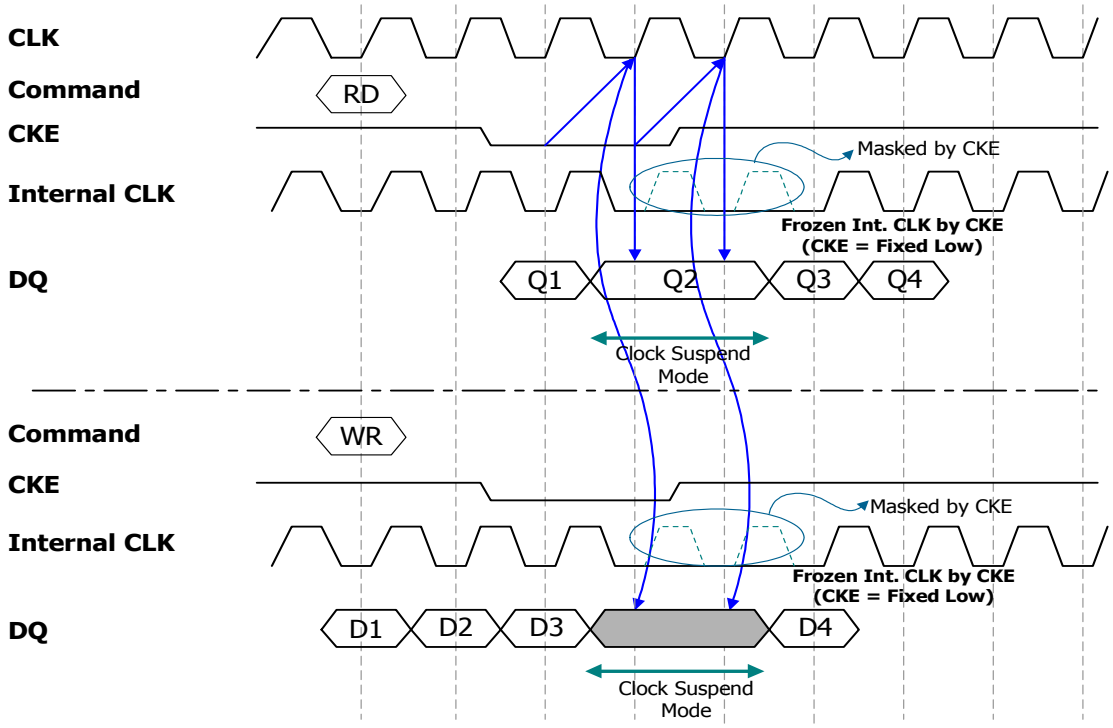

Write Data Masking




Read Data Masking

## Clock Suspend

The Clock Suspend command is used to suspend the internal clock of Mobile SDRAM. The clock suspend operation stops transmission of the clock to the internal circuits of the device during burst transfer of data to stop the operation of the device. During normal access mode, CKE is keeping High. When CKE is low, it freezes the internal clock and extends data Read and Write operations. (See examples in next Figures)



## Power Down

The Power Down command is used to reduce standby current. Before this command is issued, all banks must be pre-charged and tRP must be passed after a precharge command. Once the Power Down command is initiated by keeping CKE low, all of the input buffer except CKE are gated off.

## Auto Refresh

The Auto Refresh command is used during normal operation and is similar to CBR refresh in Conventional DRAMs. This command must be issued each time a refresh is required. When an Auto Refresh command is issued , the address bits is "Don't care", because the specific address bits is generated by internal refresh address counter.

## Self Refresh

The Self Refresh command is used to retain cell data in the Mobile SDRAM. In the Self Refresh mode, the Mobile SDRAM operates refresh cycle asynchronously.

The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled(Low). The Mobile SDRAM can accomplish an special Self Refresh operation by the specific modes(PASR) programmed in extended mode registers. The Mobile SDRAM can control the refresh rate automatically by the temperature value of Auto TCSR(Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR(Partial Array Self Refresh). The Mobile SDRAM can reduce the self refresh current($I_{DD6}$) by using these two modes.